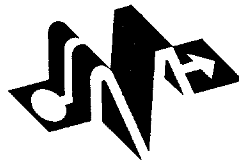
Instruction Manual
for

Model 560
Programmable
IC Tester



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INTRODUCTION

The **B & K-Precision** Model 560 Programmable IC Tester allows personnel of varied skill levels to perform fast, uncomplicated, and versatile IC testing. The powerful microcomputer-based operating system of the Model 560 allows efficiency in IC testing not previously possible with moderately-priced testers. The instrument tests over 90% of the most popular digital ICs (including many RAM and ROM ICs), due to an extensive internal library of IC test data.

To set up IC tests, you merely enter the desired testing mode, the IC generic number, and press the TEST key. The tester automatically arranges IC pin-out and test voltage levels.

The tester also has provisions for in-circuit IC testing. This is feasible via a special feature that applies current backdrive to the in-circuit IC's surrounding circuitry, allowing implementation of the tester truth table in most cases.

In addition to standard IC tests, the instrument also tests ICs contained on board assemblies where inputs of a device may be tied to logic states. Compare testing allows testing where pins may be tied to Vcc or ground; a condition that would cause "good" ICs to test "defective" with standard testing. The tester records (stores) the unique response of a reference IC and its circuit, and then uses this response for testing similar untested ICs. This feature is offered in both single-device (Device Compare) and multiple-device (Board Learn) modes. Using the Board Learn mode allows you to record the responses of all digital ICs contained on a board in one continuous operation. This mode also allows user indexing of IC and board nomenclature, thereby maintaining a convenient record of board contents for future use.

Direct, "no guesswork" IC test results are shown on the fluorescent alphanumeric display which reads "PASS", or "FAIL", showing which pin(s) tested defective. Using clear, informative directives (via the display and LED arrays), the tester guides the user through test procedures. Aural prompts are also provided to indicate the validity of an entry and device test results. These prompts allow even inexperienced users to perform tests with confidence; an important consideration in production situations where user apprehension can lead to lowered productivity.

Other time-saving features include a "retest" key that allows repetitive testing of similar ICs without re-keying the IC number or family. Also, certain keys are of the "soft" design, assuming different functions at appropriate times. This design simplifies operation by reducing the number of controls.

The Model 560 is designed with tomorrow, as well as today, in mind. Since the IC library is contained in EPROM software, periodically-expanded IC Library EPROM ICs are offered by **B & K-Precision** as new ICs are introduced. Your unit can be updated to test the newest ICs by simply replacing the library EPROMs.

An optional software package is also available which allows programming of custom devices not contained in the IC Library via a personal computer and the tester's RS-232 port.

Advanced engineering, quality construction, and user-oriented concepts and design make the Model 560 an exceptionally superior and effective instrument. To gain the most effective use of this instrument, we recommend that you study the entire contents of this manual.

MICROPROCESSOR-BASED DESIGN

Control clutter and operating difficulty is reduced because the tester operating system does the tedious work of arranging IC pinout and setting testing level. No special, or electronics knowledge is required to use the tester.

PROGRAMMED TEST SEQUENCES

User is guided through test sequences with informative prompts. If an entry error is made, the tester informs the user of the mistake allowing the user to remedy the situation.

EPROM-BASED IC LIBRARY

Built-in test sequences for over 90% of the most popular digital ICs (including many flip-flops, counters, level shifters, RAM, and ROMs) are software-based and contained on EPROM. IC library is periodically updated, making the instrument virtually obsolesence-proof.

SELF-DIAGNOSTICS PROGRAM

Proper operation of the instrument is checked each time you power-up the instrument. The self-test diagnostic program checks all internal memory, the CPU, and all pin drivers.

SELF-PROTECTION DESIGN

Logic-controlled SCR protection on all pin drivers halt the tester and float all pins in the event of an overvoltage being applied to any of the pin drivers.

20-CHARACTER DOT MATRIX VACUUM FLUORESCENT DISPLAY

Easily visible under most lighting conditions, the display indicates test results, IC entries, and user-guidance prompts in characters that are more legible than segment-type LED or LCD displays.

USER-FRIENDLY PROMPTS

Plain-English messages tell the user when to enter data. Give test results in a simple PASS/FAIL format. The user never has to interpret test data such as logic levels or truth tables. Additionally, an aural prompt reports test results and data entry validity. This allows the user to give his visual attention to the test lot instead of the tester, further enhancing throughput when performing incoming IC functional testing.

ZIF SOCKET

Zero Insertion Force out-of-circuit test socket allows quick, easy insertion and removal of devices.

RETEST KEY

Retest key allows batch testing of same-type devices without re-keying device data. Using the retest key, out-of-circuit testing can easily be done at the rate of one IC every five seconds.

IN-CIRCUIT TESTING

The tester is equipped with three test clips for testing 8 through 24 pin DIP ICs.

IN-CIRCUIT COMPARE TESTING

Compare testing allows the testing of non-standard, in-circuit applications where pins may be tied to Vcc or ground; a condition that would cause "good" ICs to test defective with standard testing. The tester records the unique response of a reference (learn) IC and uses this response for the testing of similar untested devices.

BOARD TESTING

Board assemblies containing up to 255 devices can be learned in a continuous operation. Similar boards can then be tested using the stored responses of the corresponding learn routine. Six EEPROM sockets are provided for the permanent storage of learn routines.

RS-232 PORT-EQUIPPED

RS-232 port permits User Programming of custom device test sequences using a personal computer and optional software package. Also allows connection of printer for hard-copy of test results.

SPECIFICATIONS

TEST METHOD

Internally-generated truth table test pattern stimulus. Device response logically compared to known internal response, or to user-stored reference responses.

OPERATING SYSTEM

Microprocessor-controlled with instruction set based in ROM.

CHANNELS

24 bi-directional, input/output tri-stated.

TESTING VOLTAGE

Out-of-circuit:

TTL and CMOS= 5 V.

In-circuit:

TTL= 5 V.
CMOS= 5 to 15 V (tracks circuit Vdd).

THRESHOLD LEVELS

TTL (Vcc= 5 V).

V_{IH}= 2.00 V; V_{IL}= 0.8 V.

CMOS (Vdd= 5 to 15 V).

V_{IH}= 70% Vdd; V_{IL}= 30% Vss.

DRIVER CHARACTERISTICS

Output Current:

500 mA @ maximum burst.

Test Signal Duration:

2 ms maximum.

Output Impedance:

1.5 Ω.

Output Rise/Decay Time:

200 ns.

Output Voltage Levels:

TTL:

$V_{OH} \geq 2.4$ V.
$V_{OL} \leq 0.45$ V.

CMOS:

$V_{OH} = V_{dd} - 0.1$ V.
$V_{OL} = V_{ss} + 0.1$ V.

DISPLAY

20 character dot matrix, vacuum fluorescent.

KEYPAD

Decimal keypad, membrane-type switch.

TEST SOCKET

24 pin ZIF socket.

IN-CIRCUIT TEST CLIPS

Three spring-loaded DIP test clips (16, 20, and 24 pin), each with 3 ft flat-lead cables.

PROGRAMMING

Internal:

ROM-based library containing over 90% of the most popular standard digital logic integrated circuits. See enclosed IC LIBRARY LIST for complete library. Library subject to expansion by **B & K-Precision.**

User-programmed:

1. Compare and learn modes, tester stores reference responses of device; subsequent devices are logically compared against learned reference response.
2. Optional software package allows programming of custom devices into "User Libraries" via a personal computer and RS-232 link.

USER MEMORY (Board Learn Storage)

(1) 2k x 8 RAM.
(2) 2k x 8 EEPROM, factory installed.
(4) sockets for optional 2816A 2k x 8 EEPROM, user-installed in externally-accessible compartment.

PERIPHERAL INTERFACE

RS-232 Serial port.

GENERAL

Power requirements:

Universal 100 V, 120 V, 220 V, 240 V (externally switchable) 50/60 Hz.

Operating Temperature Range:

0°C to $+50^{o}$C, RH 85%.

Storage Temperature Range:

-55°C to $+75^{o}$C, RH 85%.

Dimensions (HWD):

12.7 cm x 41.9 cm x 31.4 cm.
(5" x 16-1/2" x 12-3/8").

Weight: 9.5 kg (21 lbs).

GLOSSARY OF TERMS

Access (or Accessing)
Accessing means **a)** calling an IC generic number from the **IC Library** (using the **keypad** or **scan** keys), as to have the IC generic number appear on the display. **b)** calling a **BRD/IC** index entry (using the **keypad** or **scan** keys), as to have the **BRD/IC** index number appear on the display. Once information is **accessed**, the information is ready to be **entered.**

Board/IC index numbers
Indexing (numbering) scheme that the tester uses to maintain a record of host circuit and device nomenclature. These numbers are chosen by the user to correlate the actual board and IC numbers (e.g., "board AF-1, U108" of an example unit) of the unit under learn or test with the tester index. The two coordinating numbers that constitute an index are denoted by **BRD/IC.** Where **BRD/** appears, the manual refers to **board** index number only. Similarly, when **/IC** appears, the manual is referring only to the **IC** index number portion of the complete index.

Custom Program System
RAM and EEPROM-based memory where the user can store **Board Learn** and **Board Test** routines.

EEPROM
Electrically-Erasable Programmable Read Only Memory. Used for long-term memory of **Board Learn** and **Board Test** routines. Also used for storage of "user libraries" using optional software package. EEPROM allows convenient rewriting if user desires to re-program.

Entry
Any number or command entered into the tester by the user.

EPROM
Erasable Programmable Read Only Memory. Used for tester operating system and libraries. Contents of memory erased only with long-duration exposure to ultraviolet light, thereby ensuring security and reliability of tester operating system.

Host Circuit
Circuitry that contains (or surrounds) the in-circuit IC under test or learn.

Operating System
The ROM-based system within the instrument responsible for testing and control of all entries.

Procedure
The steps (as listed in this manual) necessary to perform a test or develop a routine correctly.

Prompt
A message issued by the tester (via the **Display** or **Aural Alert**) that informs the user of conditions during an entry or routine.

Routine
Refers to sequence of steps, from start to finish, that results in a usable **Board Learn** or **Board Test** operation.

User Library
A set of test data (truth tables and implementation patterns) that is developed by the user for custom devices not contained in the built-in EPROM IC Library. Available using optional Model AK-560 User Library Software and a personal computer.

Validate
An entry is validated when the tester accepts the entry as being **a)** correctly-placed, sequentially. **b)** within the indexing limits of the tester (as with **BRD/IC** indexes). **c)** a generic IC number entry that is contained in the IC library. **d)** within the electrical and software parameters of the tester (i.e., correct accessory EEPROM usage, in-circuit voltages within tester limits, device under test and associated circuitry allows implementation of tester logic sequence).

Verify
The tester allows clearing of any entry when entered. This allows the user to **reject** an entry if unintentional. Conversely, the user may **verify** an entry to "lock" the entry into the step being performed.

CONTROLS & INDICATORS

1. **Display.** 20 character alphanumeric fluorescent display. Displays prompts, keyboard and keypad inputs, directive commands, and test results.

2. **Keypad.** Numeric keypad used for entering IC generic number, and **BRD/IC** index numbers.

3. **Scan ↑** Key. Multi-function key used for:
   a. Scrolling up through IC library.
   b. Scanning to next higher **IC** index or **BRD** (board) index number.
   c. Selecting non-standard TTL families (i.e., L, H, LS, where applicable).
   d. Accessing overflow pin faults when number of pin faults exceed width of display.
   e. Entering RAM and ROM IC generic numbers other than 7400-series memory ICs.

   Push key to step, hold key to scroll continuously.

4. **Scan ↓** Key. Multi-function key used for:
   a. Scrolling down through IC library.
   b. Scanning to next lower **IC** index or **BRD** (board) index number.
   c. Accessing starting **BRD/IC** index numbers of a board test routine.
   d. Entering RAM and ROM IC generic numbers other than 7400-series memory ICs.

   Push key to step, hold key in to scroll continuously.

5. **Load** Key. Transfers board learn routine from EEPROM to RAM.

6. **Store** Key. Transfers board learn routine from RAM to EEPROM.

7. **DELete** Key. Allows deletion of previously-entered **BRD/IC** index pair from board learn routine.

8. **Clear RAM** Key. Clears entire RAM contents.

9. **Port ON/OFF** Key. Enables and disables RS-232 port. Turns print ON and OFF when connected to a printer. Also prepares Model 560 for "download" mode from optional User Library Software.

10. **Library Select** Key. Selects IC generic number prefix (**74---**, **4---**, **40---**, **9---**, **14---**, **M ➡**). TTL or CMOS logic level is automatically set. By pressing key, tester steps through libraries (including any optional "user libraries"), returning to TTL library after all possible choices are cycled through. Library selection is indicated on **Display** and **Input Level LED Array** as follows:

> Sample prompt (TTL families):
> **ENTER IC #: 74**
> (**TTL** LED is lit)
>
> Sample prompt
> (CMOS 4000-series family):
> **ENTER IC #: 4**
> (**CMOS** LED is lit)

11. **REVise** Key. Allows IC revision in a previously-compiled **BRD/IC** index.

12. **INSert** Key. Inserts and validates entry in **board learn** mode.

13. **Enter** Key. Checks validity of entry, and enters data into tester if entry is valid.

14. **Clear Entry** Key. Clears preceding entry if mistake was made.

15. **Input Level** Key. Selects CMOS logic level for testing TTL-pinout (74C-series) CMOS ICs. Pressing **Input Level** key once activates TTL(C) testing level when TTL library is selected. Press **Input Level** key again to return to standard TTL logic level. Selection indicated by **Input Level LED Array.**

16. **TEST** Key. Multi-function key with the following functions:
    a. Tests entered device in the **Device Test** and **Board Test** modes.
    b. Stores reference IC response in the **Board Learn** or **Device Compare** modes.

17. **IN CKT/OUT CKT** Key. Selects in-circuit or out-of-circuit testing. Automatically steps to **OUT CKT** in **Device Test** mode upon power-up. Automatically steps to **IN CKT** for all other modes. Setting is indicated by **Mode Status LED Array.** May be set as desired for all test modes.

18. **Mode Clear** Key. Multi-function key with the following functions:
    a. Clears presently-selected mode, allowing for mode change.
    b. Resets tester to test different ICs in **Device Test** and **Device Compare** modes.
    c. Resets tester in **Board Test** mode, allowing for access of next **BRD/IC** index of board test routine.

19. **Retest** Key. Allows direct retest of same-type, same number IC by pressing key, then press **TEST** key.

20. **Mode Select** Key. Selects testing mode. By pressing key, tester steps through four modes as follows:

    Device Test

    Device Compare

    Board Test

    Board Learn

    Selected mode is indicated by **Mode Status LED Array.**

21. ⏚ **Lead Jack.**

22. ⏚ **Clip.**

23. **In-Circuit Test Cable/IC Test Clip.**

24. **Test Cable Connector.**

25. **IC Test Socket.** 24-pin ZIF socket. Allows easy insertion and removal of IC when **Socket Lever** is unlocked, while providing positive electrical contact when **Socket Lever** is locked.

26. **Socket Lever.** Locks and unlocks IC into socket.

27. **EEPROM Compartment.** Easy-access compartment containing four **custom program sockets** for optional 2k x 8 EEPROMs.

28. **Mode Status LED Array.** Indicates mode of operation when corresponding LED is illuminated.

    DEVICE TEST LED. Indicates **device test** mode is selected.

    DEVICE COMPARE LED. Indicates **device compare** mode is selected.

    BOARD TEST LED. Indicates **board test** mode is selected.

    BOARD LEARN LED. Indicates **board learn** mode is selected.

    OUT CKT LED. Indicates tester is set for out-of-circuit testing.

    IN CKT LED. Indicates tester is set for in-circuit testing.

29. **Input Level LED Array.**

    TTL LED. Indicates TTL family Library is seleced (i.e., 74/54-series generic IC number prefix).

    CMOS LED. Indicates CMOS family Library is selected (i.e., 4000, 40000, 14000-series CMOS, 74(C)-series TTL-configured CMOS, etc).

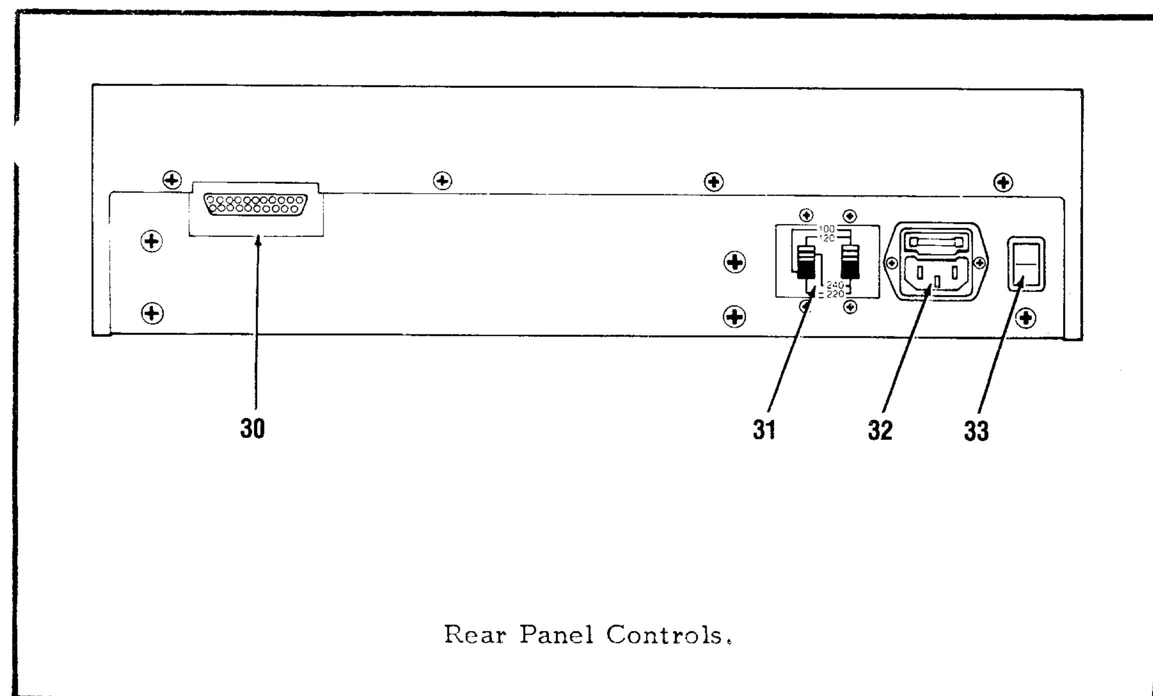
30. **RS-232 Port.** Standard RS-232 port. 25-pin "D" connector.

31. **Line Voltage Selector Switches.**

32. **Line Cord/Fuse Receptacle.**

33. **POWER Switch.** Turns tester **ON** and **OFF.**

34. **Aural Alert** (not shown). One beep indicates a valid entry, while three beeps in rapid succession indicates an invalid entry or step. Three beeps also indicates "IC tests defective" after **TEST** key is pressed.



Rear Panel Controls.

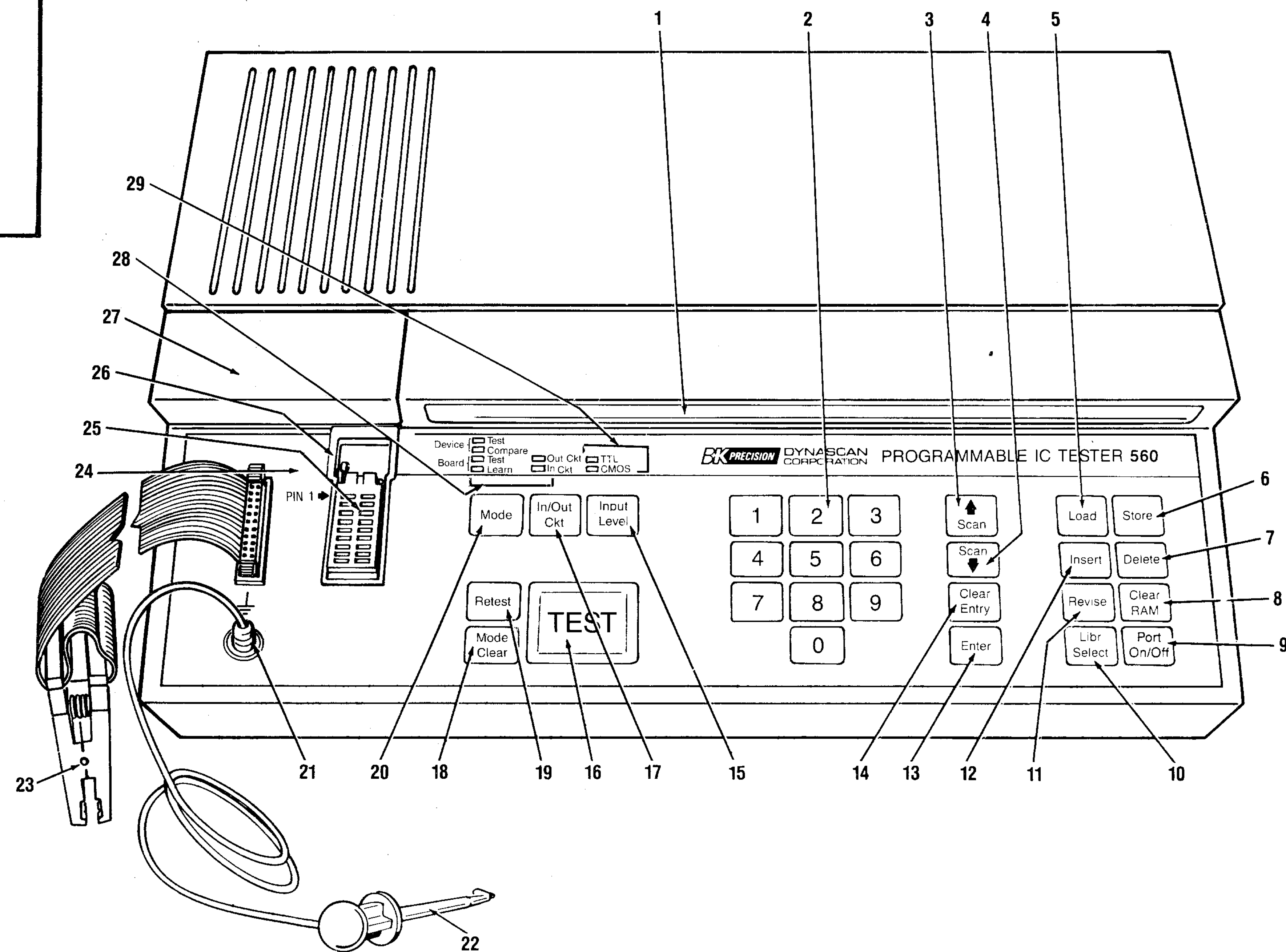


Fig. 1. Front Panel Controls & Indicators.

This section of the manual contains the general operating instructions that are used with **all** test modes. In addition, there are individual sections with complete step-by-step operating instructions for each mode of operation. To enhance clarity, the information given in this section is not repeated in detail in the individualized sections.

SAFETY PRECAUTIONS

WARNING

The following precautions must be observed to help prevent electric shock.

1. Observe all safety precautions listed in the TEST INSTRUMENT SAFETY section of this manual.
2. Keep hands free from line voltage and high voltage areas when connecting test clip to in-circuit devices.

EQUIPMENT PROTECTION PRECAUTIONS

CAUTION

The following precautions will help avoid damage to the test instrument.

1. The tester is protected against damage from voltages up to ±18 V that may be applied to the **IC Test Clip. Do not** connect the **IC Test Clip** to a portion of circuit where in-circuit voltages may exceed ±18 V.
2. Only connect the **IC Test Clip** to a logic IC.
3. Only connect the RS-232 port to equipment which is formatted and designed for termination into an RS-232 port.
4. When inserting an EEPROM into a **CUSTOM PROGRAM** socket, make certain that the EEPROM is properly inserted and locked before powering-up tester. **Never** insert or remove an EEPROM with the tester powered-up.

CORRECT OPERATING PRACTICE

NOTE

The following conditions must be observed to ensure correct operation of the tester.

1. Power-up tester **before** connecting tester to in-circuit device. While no tester damage will occur if this is not observed, the tester will enter a self-protection mode, requiring the user to correct the condition and power-up again.
2. The **IC Test Socket** and **IC Test Clip** share common pin connections within the tester and, therefore, are **not** electrically independent of each other. If the **IC Test Clip** is used, make certain **IC Test Socket** is **empty.** Likewise, the **IC Test Clip** should not be connected to a device if the **IC Test Socket** is intended for use.
3. Under conditions where an invalid entry or procedure is attempted, the tester responds with an error prompt accompanied by a three-beep aural alert. If any such prompts occur, detailed description of the message and corresponding remedial action is given in the SPECIAL PROMPTS section of this manual.

TESTER POWER-UP

1. Set **POWER** switch to **ON** position (power switch is located on rear panel of instrument). When tester is **ON,** the tester executes a self-diagnostic test routine,

during which the tester will verify proper operation of internal memory and pin drivers and display the message:

DIAGNOSTIC TEST....B & K-PRECISION MODEL 560 Ver_._ SELF-TEST OK (Version number displayed depends upon installed system software version)

2. Once the self-diagnostic routine is complete, the tester automatically steps to the **TTL, OUT CKT, Device Test** mode.

3. At this time, the tester is ready to accept TTL IC entries in the **TTL, OUT CKT, Device Test** mode; or the mode may be changed as desired.

USING IC TEST SOCKET
(Refer to Fig. 2)

The Model 560 is equipped with a ZIF (Zero Insertion Force) socket that offers fast and easy IC testing, as well as reducing the chance of IC lead bending or breakage. To properly insert or remove an IC, use the socket as follows:

CAUTION

Do not attempt to insert or remove IC from test socket when ***socket lever*** *is in locked position. IC and/or test socket damage will occur if this is attempted.*

1. Make certain **IC Test Clip** is disconnected from any device.
2. Unlock the **socket lever** (lever up).
3. Insert IC into socket so that pin 1 of IC aligns with the **PIN 1** mark on test socket, as indicated on front panel.
4. Lock IC in test socket (lever down).
5. After test, place **socket lever** in the unlocked position (lever up) and lift IC from test socket.

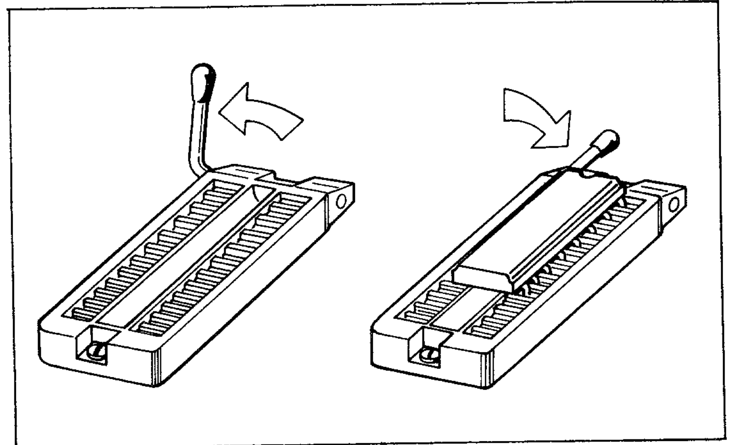


Fig. 2. Using IC Test Socket.

USING IN-CIRCUIT TEST CABLE
(Refer to Fig. 3)

NOTE
Read "In-Circuit Considerations" items in the TIPS & HINTS TO HELP AVOID COMMON MISTAKES section before performing an in-circuit test.

1. Remove any IC from **IC Test Socket.**
2. Make sure red stripe on test cable aligns with **PIN 1** marker on instrument **test cable connector.**
3. Press test cable firmly into front panel **test cable connector.** A "click" is heard when cable is locked into instrument. Connector will only fit when properly oriented.
4. Place **IC Test Clip** over IC under test by expanding clip jaw and placing over IC. Note the following conditions:

   a. Make certain red **PIN 1** marker on test clip is aligned with pin 1 of IC.

b. Make certain that the test clip is completely positioned over all leads of the IC under test. As indications, a correctly positioned test clip will touch the PC board or IC socket and will easily stay attached to the IC under test.

c. Since the tester applies a very small signal to the IC under test, **a good electrical connection between the IC under test and the test clip is mandatory.** With test clip positioned over IC under test, wiggle the test clip a small amount from side-to-side before proceeding. This ensures a good electrical connection.

CAUTION

*Inside the tester, the ⏚ **clip** is connected to earth ground. Therefore, the ⏚ **clip** connection point on the circuit under test must also be referenced to earth ground; or be isolated from earth ground. Otherwise damage may result to equipment under test.*

5. Connect ⏚ **clip** to chassis ground point in circuit under test. This point must be electrically related to the Vcc supply of the device(s) under test.

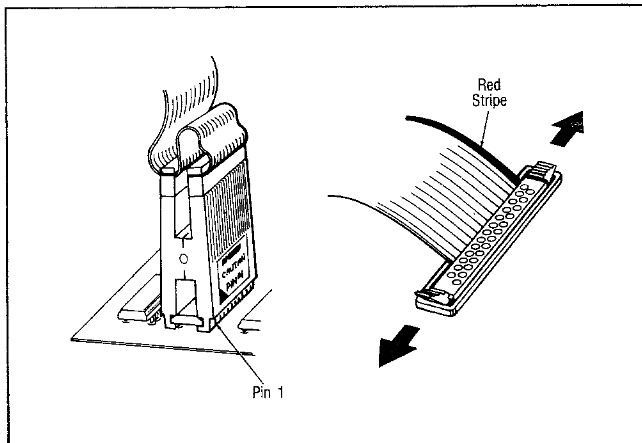


Fig. 3. Using IC Test Clip.

6. Disconnect test cable from front panel connector by pushing connector locks away from center of connector, while gently pulling cable.

SELECTING IC FAMILY/TYPE

1. Select desired IC family using **Library Select** key:

   74/54-series TTL

   4000-series CMOS

   40000-series CMOS

   9000-series

   14000-series CMOS

   Memory ICs

   Optional "User Libraries"

   Selection is indicated by the **Display** prompt and **Input Level LED Array.** Tester is automatically set to TTL library when powered-up. For each press of **Library Select** key, another family is accessed. After all family choices are scanned through, library goes back to TTL.

2. For 74(C)-series level, press **Input Level** key once. Press **Input Level** again to revert to standard TTL library.

NOTE

When testing certain TTL-numbered ICs where the SELECT FAMILY prompt occurs, note the following consideration: HCT, HCT, and HCU ICs, while being of CMOS design, should be tested under the TTL family selection.

3. **TTL Family Select** prompt occurs with certain TTL ICs, such as the 74LS55 and 74H85. This is due to pinout differences used among 74/54 family types.

Display Prompt:
(SELECT FAMILY: TTL Std)

a. If prompt occurs, press **Scan** ▲ key once to access each non-standard family, as shown below:

Example Display Prompts:

(SELECT FAMILY: LS)

(SELECT FAMILY: L)

(SELECT FAMILY: AS)

After all possible non-standard choices for the entered device are cycled through, the prompt reverts to standard **(Std)**.

NOTE

There is no functional ("truth table") difference between the 74-series and 54-series TTL families. 54-series ICs differ from 74-series ICs only in that 54-series ICs meet more stringent specifications regarding environmental and absolute ratings. Enter 54-series ICs as you would enter 74-series ICs.

b. After selecting desired family, press **Enter** key again to verify selection.

USING SCAN ▲ ▼ KEYS

Using the **Scan** keys saves time and simplifies operation in many cases.

Entering IC Generic Numbers

After selecting the appropriate IC library, press the **Scan** ▲ key or **Scan** ▼ key to find the IC generic number you wish to enter. Upon accessing the desired generic number, press the **Enter** key and entry is immediately validated. The entered IC is ready for test.

Entering BRD/IC Numbers (Board Test Mode)

1. Hold the **Scan** ▼ to access the first (lowest-numbered) **board test** index. Press **Enter** to enter **BRD/IC** index number.

2. After test of any **BRD/IC** index, pressing either **Scan** key at the time of the next **BRD/IC** index entry returns you to the previously tested index number, thereby maintaining your place in the routine.

Entering RAM/ROM IC Numbers (other than 74-series)

Scan keys are also used for entering certain RAM and ROM IC generic numbers. Refer to TESTING MEMORY ICs section of this manual.

TEST RESULT PROMPTS

(excluding memory ICs)

1. The Model 560 indicates IC functional test results in a PASS/FAIL manner with no interpretation of data, logic levels, or truth tables being necessary.

2. If the truth table obtained from the IC under test matches the reference truth table for that IC, the tester issues the following prompt:

Display Prompt:

(RESULT: PASS)

3. If the truth table obtained from the IC under test **does not match** the reference truth table for that IC, the tester issues the following prompt:

Display Prompt:

(RESULT: FAIL)

When an IC reads "FAIL", the tester also indicates at which pins the defect was noted, as shown below:

Display Prompt:

(PIN: n)

n= Pins where defect was noted.

4. Refer to TESTING MEMORY ICs section for RAM and ROM test instructions.

USING RETEST KEY

The **Retest** key allows immediate re-entry of a previously-tested IC generic number, allowing additional testing of same-type devices by pressing only two keys. Use this feature for incoming QC inspection where ICs of the same generic number are tested repeatedly. Usage of this feature is given in the following steps:

1. Remove the previously-tested device from the **IC Test Socket** (or remove **IC Test Clip**).
2. Connect the tester to another same-type device.
3. Press the **Retest** key. The tester is now ready to test untested device. Press **TEST** key to test device.
4. Repeat the three previous steps for additional same-type (same generic number) devices.

AURAL PROMPTS

The tester issues aural prompts to further enhance simplicity of testing. One "beep" indicates a valid entry, or "RESULT: PASS". Three "beeps" indicate an invalid entry (such as a generic IC number not in library or a programming sequence error) or "RESULT: FAIL".

Because the contents (output logic) of RAM and ROM ICs is not "fixed", or predetermined (as in the case of combinational logic ICs) these ICs cannot be tested using a predetermined truth table held in the tester's IC Library.

The Model 560 tests RAM ICs by writing in to the RAM with a known contents. Immediately following the write operation, the contents are read back while the tester looks for mismatches.

ROM ICs are typically user-programmed with data that is valuable. Therefore, the tester checks ROM ICs by reading the ROM contents and performing a "checksum".

> Memory ICs are tested using the same steps as given for standard ICs in this manual. Follow the section that corresponds to the testing mode you intend to use (e.g., "Out-of-Circuit Device Test Mode, "In-Circuit Device Test Mode", etc). The only differences while following the standard steps are as follows:
>
> **Certain memory ICs are entered using only the scan keys.**
>
> **The TEST RESULT prompts issued by the tester are different for memory ICs, as compared to other ICs.**
>
> These differences are discussed below in separate sections.

ENTERING RAM and ROM IC GENERIC NUMBERS

74-series RAM and ROM ICs are entered the same way that other 74-series IC generic numbers are entered: The suffix digits are manually entered using the **keypad,** or the suffix digits may be scrolled to using the **Scan ▲** or **Scan ▼** keys.

However, RAM and ROM IC generic numbers **that do not have a 74— prefix** are contained in a separate library and accessed using the **Scan** keys only. These memory ICs are listed below:

2114		2115
2142		2147
2148		2167
2716	6116	2732

The IC types listed above are entered as follows:

1. Select **Test Mode** and connect tester to IC under test as outlined in the GENERAL OPERATING INFORMATION and TEST MODE sections of this manual.

2. Repeatedly press the **Library Select** key until the following prompt indicating MEMORY Library selection is displayed:

> Display Prompt:
>
> **ENTER IC#: M ▶**

3. Repeatedly press the **Scan ▲** key until the desired device number is displayed. If you pass the desired number, use the **Scan ▼** key.

4. When the desired device number is displayed, press **Enter.**

5. Press **TEST** key to test or obtain checksum.

RAM TEST RESULT PROMPTS

RAM ICs are tested by the Model 560 in the following manner: All address locations of a RAM are written with pre-determined contents. The Model 560 reads back each address location and compares the read-back contents to the pre-determined write contents.

1. Press the **TEST** key.

2. If the read-back contents compare exactly with the pre-determined contents, the IC is declared functionally passing. In this case, the following prompt is displayed:

> Display Prompt:
>
> **RESULT: PASSED**

3. If any of the read-back contents **do not compare** with the pre-determined contents, the tester notices this mismatch and issues the following prompt:

> Display Prompt:
>
> **RESULT: FAIL ADDR nnnn**
>
> nnnn = address location where mismatch was noted

TESTING ROM ICs

The data contents of a ROM IC are typically programmed via custom programming performed by the user. In other words, the contents of a ROM **are entirely dependent on the data that is programmed into the ROM.** The Model 560 and other non-custom IC test instruments cannot determine the "correct" contents of a given ROM, since this information is entirely arbitrary and totally related to the program contained by the ROM.

The Model 560 tests ROM ICs by performing a "checksum" operation on a ROM under test.

Checksum is the summation of the contents held in each memory location of a given ROM. An example ROM IC and its checksum is shown below:

Memory Location (hex)	Contents at that address (hex)
0000	0008
0001	0009
CHECKSUM =	$8_H + 9_H = \mathbf{11_H}$

A **purely arbitrary example** prompt is shown below:

> Display Prompt:
>
> **RESULT: CHKSUM 19EF**

The checksum obtained from the Model 560 checksum operation is compared to the known checksum for the program written on the IC. The checksum is displayed in four-digit hexadecimal. If the checksum obtained from the tester matches the known checksum for the given ROM, the ROM can be considered passing.

If the expected checksum for a given ROM is not known, other identical ROMs with identical programming may be used as a reference to establish a known checksum.

1. Press the **TEST** key.

2. Note the checksum obtained from the Model 560 checksum operation and compare this to the known checksum for the program written on the IC. If checksum is not equal to known checksum, ROM can be considered defective.

3. Depending on ROM type and the contents programmed on the ROM, checksums may exceed four hex places. In these cases, the four least significant digits (LSD) of the checksum are displayed.

4. During **Board Learn**, ROM checksums are stored and used as a reference for other identically-programmed ROMs. Using **Board Test**, RESULT: PASS or RESULT: FAIL test prompts are issued.

TIPS & HINTS TO HELP AVOID COMMON MISTAKES

GENERAL CONSIDERATIONS (use with all testing)

1. When powering-up the tester, make certain the **Test Socket** has no IC in it. Also make certain that the **IN-CKT Test Clip** is not connected to the tester.

2. 40-series and 4-series CMOS ICs are accessed using different IC Libraries. **The "rule of thumb" is as follows:**

   If the IC number starts with a "4" and is **four digits long**, use the **ENTER IC#: 4—** Library.

   If the IC number starts with a "4" and is **five digits long**, use the **ENTER IC#: 40—** Library.

3. If a printer is used, press the **Mode Clear** key after the last test result is taken. Some printers store the last line of print in a buffer. Pressing the **Mode Clear** key ensures that the last line of print will exit the buffer and be printed.

4. Whether using the **Test Socket** or **IN CKT Test Clip,** make certain that no protective coating remains on the IC pins. When shipped new, some IC manufacturers apply a non-conductive, anti-oxidant to the pins.

IN-CIRCUIT CONSIDERATIONS

5. The PC board under test ("host circuit") must be powered-up. The tester uses an earth ground reference. If the common of the circuit under test is not at earth ground, the circuit must be isolated to prevent damage.

6. A good connection between the **IN CKT Test Clip** and the IC is a must. A poor connection will not allow a reference IC to be learned properly, as well as not allowing proper testing of an untested IC. The Model 560 is equipped with the best quality DIP test clip available. The limited spring tension used by the test clip is necessary in order to avoid damaging the IC. The following tips help avoid mistakes when using the test clip:

   a. With the test clip positioned on the IC, wiggle the test clip from side-to-side a small amount. This helps seat the test clip contacts against the IC pins.

   b. Cleaning the exposed portion of the IC pins with a pencil eraser helps ensure a positive electrical connection between the test clip and IC. **This is especially important if the circuit has been in service for a long time** and oxidation is present on the IC pins. Also, no trace of soldering flux should remain on the IC pins.

   c. Make certain that the test clip is symmetrically positioned over the IC. The test clip should be facing straight-up when connected to the IC.

   d. Make certain that the test clip is positioned over **all** IC pins. This can be done by ensuring that the **PIN 1** marker on the test clip mates with pin 1 of the IC.

7. Disable all circuit clocks before testing.

8. When using the **IN CKT Device Test** mode, "good" devices may test falsely as "defective" under certain conditions. This situation can occur if the device has logic inputs tied to a certain state (i.e., unused inputs tied to Vcc or ground). If a logic input is tied to a certain state, the tester cannot logically "toggle" the input HIGH and LOW; this, in effect, prevents that input of the device from responding

to the tester truth table implementation. If this occurs, the **Device Compare** and **Board Learn** modes permit testing.

9. Since the **Device Compare** and **Board Learn** modes consider the learned response a function of the IC as well as associated external logic signals, comparison testing is valid only when testing ICs of the same generic number, hosted by identical circuitry. That is, invalid test results may occur when testing identical ICs in dissimilar circuitry.

10. It is recommended that the power supply of the circuit under test possess adequate current capabilities and overload protection for in-circuit testing. When an in-circuit voltage exceeds the ±18 V safe limit of the tester, the protection feature of the tester "clamps" the affected line. This clamping presents a low dc resistance to the Vcc supply of the circuit under test. Host circuit power supplies with marginal current capabilities may be overloaded during this condition, causing the host circuit power supply fuse to blow. For TTL circuits, the **B & K-Precision** Model 1625 5 Volt, 10 Amp DC Power Supply is highly suited for use with Model 560 in-circuit testing.

11. Make certain any tri-state buffers or latches connected to address or data busses are in the "HI-Z" state before testing any IC.

12. When developing a learn routine on a circuit, it is a good idea to perform a repeatability test on the reference circuit (i.e., test the circuit immediately after the learn routine). Ideally, when a circuit is learned, a repeated test of the same circuit should give a "TEST: PASSED" result for every IC of the learn routine. If a "TEST: FAIL" result occurs during the repeat test, is most probably means that the test clip was not properly connected to the IC where a "TEST: FAIL" prompt occured.

13. Inside the tester, the ⏚ **clip** is connected to earth ground. Therefore, the ⏚ **clip** connection point must also be referenced to earth ground, or be isolated from earth ground.

14. The tester is designed for circuits using positive logic (i.e., "1"= +V, "0"= 0V). If **IN CKT** testing is selected and the circuit under test uses negative logic, the circuit under test must use a floating ground (i.e., logic supply ground floated from chassis ground or "earth").

15. TTL ICs are tested at 5 volts Vcc. For CMOS families (**IN CKT**), the tester senses the Vcc of the circuit under test and adjusts tester Vcc to the same value. There is no need to adjust CMOS in-circuit voltages for testing.

OUT-OF-CIRCUIT DEVICE TEST MODE

The **out-of-circuit (OUT CKT) Device Test** mode is most useful for incoming QC batch testing, or for circuit assemblies where the ICs are removable and out-of circuit testing is desired. Follow all instructions given in the GENERAL OPERATING INFORMATION section of this manual.

NOTE

Refer to TIPS & HINTS TO HELP AVOID COMMON MISTAKES section of this manual before performing test for first time.

1. Set **POWER** switch to **ON.**

2. Insert IC into **IC Test Socket.** Make certain pin 1 of IC corresponds to **PIN 1** marker on test socket.

3. **Test mode** is automatically set to **Device Test/OUT CKT** when tester is powered up; no control changes are necessary. If tester is powered-up and another mode was in use, select **Device Test** at this time.

4. Select IC family (type) that matches family of IC under test using the **Library Select** key and **Input Level** key.

5. Enter the IC generic number using the **keypad** or **Scan** keys and press **Enter** to verify entry. Press **Clear Entry** to clear wrong entry. Clearing entry will not return tester to initial stage of procedure; simply re-enter suffix digits again.

6. If **Family Select** prompt occurs, press the **Scan**▲key to select family type (e.g., L, LS, H, ALS, F). Press the **Enter** key again to verify selection.

7. Tester is now ready to test IC, as indicated by following prompt:

> Display Prompt:
>
> (**RDY TO TEST** 7400)
>
> 7400 = example generic IC number entry

8. Press the **TEST** key to test IC.

9. After the **TEST** key is pressed, the tester indicates whether the IC is good or defective with the following prompts:

> Display Prompt:
>
> (**RESULT: PASS**)
>
> Display Prompt:
>
> (**RESULT: FAIL**)
>
> (**PIN:** 4,8)
>
> 4,8= Pins (example) where fault was detected. If arrow is present at right hand side of display, more pin faults were detected than could be presently displayed; press **Scan** ▲ key to display additional pin fault detections.

10. For RAM and ROM ICs, refer to TESTING MEMORY ICs section of this manual.

11. Use the **Retest** key to test additional devices of the same generic number.

12. Press the **Mode Clear** key to allow testing of different IC types, or to change mode. Select other modes using **Mode Select** key.

IN-CIRCUIT DEVICE TEST MODE

The **in-circuit (IN CKT) Device Test** mode is useful for testing ICs that cannot be easily removed from the host circuit, such as encountered when testing assemblies returned for service.

NOTE

The following **special prompts** may be encountered using this procedure. Consult SPECIAL PROMPTS section of manual if further information is necessary.

(**Insufficient Vcc**)

(**WARNING! INPUT EXCEEDS 16.5 V**)

(**TTL OVERVOLTAGE**)

(**CAN'T RESET DEVICE**)

NOTE

If device under test has logic inputs "hard-wired" to Vcc or ground, a test result of "defective" will occur regardless of IC condition. If this situation is encountered, use a compare-type test, such as offered using the **device compare** mode, or the **board learn & test** modes.

Refer to TIPS & HINTS TO HELP AVOID COMMON MISTAKES section in this manual before performing test for the first time.

1. Set **POWER** switch to **ON.**

2. Connect **IC Test Clip** to in-circuit IC. Make certain **PIN 1** marker on test clip corresponds to pin 1 of IC under test.

3. Connect the ⏚ **clip** to a chassis ground point on the circuit under test.

4. Disable all clock signals on circuit under test.

5. Power up the circuit under test.

6. **Test Mode** is automatically set to **Device Test** when tester is turned on. If tester is already powered-up and another mode was in use, select **Device Test** mode at this time.

7. Press **IN CKT/OUT CKT** key until **IN CKT** LED lights.

8. Select IC family (type) that matches family of IC under test using the **Library Select** and **Input Level** keys.

9. Enter the IC generic number using the **keypad** or **Scan** keys and press **Enter** to verify entry. Press **Clear Entry** to clear wrong entry. Clearing entry will not return tester to initial stage of procedure; simply re-enter suffix digits again.

10. If **Family Select** prompt occurs, press **Scan ⇑** key to select family type (e.g., L, S, H, ALS, F). Press **Enter** key again to verify selection.

11. Tester is now ready to test IC, as indicated by the following prompt:

Display Prompt:
(**RDY TO TEST 74153**)
74153 = example IC generic number entry

12. Press **TEST** key to test IC.

13. After the **TEST** key is pressed, the tester indicates whether the IC is good or defective with the following prompts:

Display Prompt:

(RESULT: PASS)

Display Prompt:

(RESULT: FAIL)

(PIN: 4,8)

4,8= Pins where fault was detected. If arrow is present at right hand side of display, more pin faults were detected than could be presently displayed; press **Scan** ▲ key to access additional pin fault detections.

14. For RAM and ROM ICs, refer to TESTING MEMORY ICs section of this manual.

15. Use the **Retest** key to test additional devices of the same generic number.

16. Press the **Mode Clear** key to allow for test of different IC types, or to change mode. Select other modes using **Mode Select** key.

DEVICE COMPARE MODE

The **Device Compare** mode is useful for testing in-circuit ICs where logic inputs of the IC are tied to fixed states (i.e., inputs "hard-wired" to Vcc or ground), thereby preventing the tester from applying its standard device test sequence. This mode circumvents such conditions by recording the logic response of a known good device and host circuit; the stored response is then used as the reference response for testing same-type devices hosted by identical circuitry.

NOTE

Refer to TIPS & HINTS TO HELP AVOID COMMON MISTAKES section of this manual before performing test for the first time.

The following **special prompts** may be encountered using this procedure. Consult SPECIAL PROMPTS section of manual if further information is necessary.

(**Insufficient Vcc**)

(**WARNING! INPUT EXCEEDS 16.5 V**)

(**TTL OVERVOLTAGE**)

(**CAN'T RESET DEVICE**)

1. Set **POWER** switch to **ON.**
2. Make certain **PIN 1** marker of test clip correspond with pin 1 of IC under test.
3. Connect the ⏚ **clip** to a chassis ground point.
4. Disable any clocks on circuit under test.
5. **Make absolutely certain that the reference IC and circuit used for response recording are fully functional,** as this unit will be the standard for subsequent similar units. It is good practice to perform a complete learn/test cycle on the reference device in order to verify that the reference circuit permits valid testing.
6. Using **Mode Select** key, set **Test Mode** to **Device Compare.**
7. Tester automatically sets **IN CKT/OUT CKT** to **IN CKT** upon selecting **Device Compare** mode.
8. Select IC family (type) that matches family of IC under test using the **Library Select** and **Input Level** keys.
9. Enter the IC generic number using the **keypad** or **Scan** keys and press **Enter** to verify entry. Press **Clear Entry** to clear wrong entry. Clearing entry will not return tester to initial stage of procedure; simply re-enter suffix digits and press **Enter** key again.
10. If **Family Select** prompt occurs, press **Scan**▲ key to select family type. Press **Enter** key again to verify selection.
11. Tester is ready to record the device response, as indicated by the following prompt:

Display Prompt:
(**RDY TO RECD 4011**)
4011= example IC generic entry

12. Press the **TEST** key. The reference logic response of the device under test is now recorded.
13. The tester is now ready to test identical devices hosted by identical circuitry, as indicated by following prompt:

Display Prompt:

(RDY TO COMPARE)

14. Remove **IC Test Clip** from reference IC and connect test clip on IC to be tested.

15. Press **TEST** key to execute **compare** of device under test. Compare result is indicated by display and aural prompts.

Display Prompt:

(RESULT: PASS)

Display Prompt:

(RESULT: FAIL)

(PIN: 4,8)

4,8= Pins where fault was detected. If arrow is present at right hand side of display, more pin faults were detected than could be displayed; press **Scan** ▲ key to access additional pin fault detections.

16. For RAM and ROM ICs, refer to TESTING MEMORY ICs section of this manual.

17. Use the **Retest** key to test additional devices of the same generic number, hosted by identical circuitry.

18. Press the **Mode Clear** key to allow for test of different IC types, or to change mode. Select other modes using **Mode Select** key.

BOARD LEARN MODE

The **Board Learn** mode is useful for in-circuit testing where more than one IC per circuit board requires testing. The testing sequence used here is similar to device compare; a reference response is stored in RAM and used for comparison testing of additional devices of the same type, hosted by identical circuitry. However, this mode allows for the response storage of many ICs in one continuous operation (**routine**). Additionally, the **board learn** mode provides a built-in means of keeping a record of IC generic number and user-assigned nomenclature for each IC in the routine (**indexing**). In other words, the board learn mode allows you to "keep track" of the IC responses recorded in a routine by allowing you to enter a "board number" and "IC number" along with the IC generic number. The "board number" can be the part number of the board, while the "IC number" can be the schematic number or silkscreened IC number on a PCB that correlates an IC generic number. Any time a stored IC in a routine is accessed, the **display** prompts with the IC generic number, as well as the "board" and "IC" index numbers, reminding the user of their entry. The index you compile using this mode correlates the testing sequence of additional, identical untested units with the sequence used during the reference (learn) routine. Furthermore, board learn routines can be stored in permanent memory (EEPROM) and recalled (loaded) whenever desired.

NOTE

Routines compiled in the **board learn** mode are stored in RAM (temporary memory) while being compiled. **Any time tester power is interrupted, the RAM contents will be lost.** If a **board learn/board test** routine is intended for use at a later time, the **learn** portion of the routine must be stored in user EEPROM before turning **POWER** switch off. Make certain EEPROM is installed before performing routine, since tester power must be OFF before installing EEPROM IC. Refer to MEMORY TRANSFER and CONTROL section of this manual for instructions on storing routines.

Refer to TIPS & HINTS TO HELP AVOID COMMON MISTAKES section of this manual before performing learn routine for the first time.

The following **special prompts** may be encountered using this procedure. Consult SPECIAL PROMPTS section of manual if further information is necessary.

ALREADY STORED

Insufficient space

Insufficient Vcc

RAM EMPTY

TTL OVERVOLTAGE

WARNING! INPUT EXCEEDS 16.5 V

1. Set **POWER** switch to **ON**.
2. Connect the **IC Test Clip** to in-circuit IC. Make certain **PIN 1** marker on test clip corresponds to pin 1 of reference IC.
3. Connect the ⏚ **clip** to a chassis ground point on the reference host circuit.
4. Disable all clocks on reference host circuit.
5. Power up the reference host circuit.
6. The tester uses an indexing scheme consisting of board (**BRD**) and IC (**IC**) numbers.

a. Choose "board" (**BRD**) and "IC" (**IC**) index numbers that correlate your host circuit nomenclature to the tester "**BRD**" and "**IC**" indexing scheme. Typically, the **BRD** index number you choose should reflect the PCB number of the learn circuit; the **IC** index number you choose should be the schematic number or number screened on the circuit board.

b. The numbers you choose can be arbitrary, as long as they are recorded and correlate to the host circuit (i.e., "tie" the IC generic number back to the host circuit). This is important because the tester will record and validate any index numbers entered during the **board learn** mode. Therefore, the possibility of confusing the tester **BRD/IC** index numbers with your circuit's nomenclature can be avoided when testing other similar circuits if an indexing system is used.

c. Noting the nomenclature of your circuit board and the chosen index numbers, make photocopies of the BOARD LEARN/TEST LOG SHEET form found at the end of the manual. Fill in the sheet with the **BRD, IC,** and IC generic numbers used with the learn circuit.

An example board and application of the recommended theme is shown in Fig. 4.

7. **Make absolutely certain that the reference IC and host circuit used for response recording is fully functional,** as this unit will be the standard for untested similar units. Perform a board test routine on the reference circuit to check response validity.

8. Using the **Mode Select** key, set **Test Mode** to **Board Learn.** Tester is automatically set to **IN CKT** when this mode is selected.

Unit Nomenclature:	560 Index No:
Model # PCB # IC generic #	**BRD- / IC-**
XN1000 PCB 121 U101= 7400	121/101
XN1000 PCB 121 U102= 74LS54	121/102
XN1000 PCB 250 U210= 4011	250/210

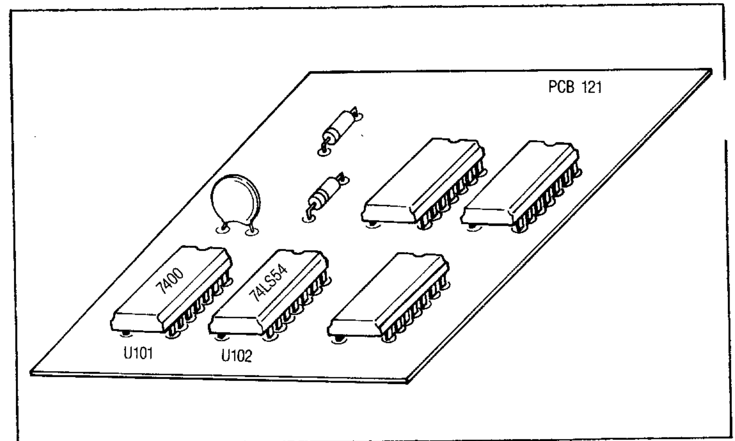


Fig. 4. Board/IC Index Correlation Theme.

9. Tester requests a board index number (**BRD**) with the following prompt:

Display Prompt:
(BRD)

10. Using the **keypad**, enter a board index number (**BRD**). Board and IC index numbers up to 255 are permitted. If you exceed this limit, the tester prompts with a three "beep" aural error prompt.

11. Verify the entry by pressing the **Enter** key. If a different board index number is desired, cancel the entry with the **Clear Entry** key and re-enter desired number.

12. After verification of the board index number, the tester requests an IC index number (**IC**) with the following prompt:

Display Prompt:
(BRD 1 **IC**)
1= example board index number

13. Enter the **IC** index number using the **keypad.** Verify the entry by pressing the **Enter** key. If a different IC index number is desired, cancel the entry by pressing the **Clear Entry** key; re-enter intended number.

14. The tester now displays the following prompt:

Display Prompt:
(**INS/REV/DEL ?**)

At this point, the tester needs to know whether the **BRD/IC** entry is new (never entered before in this routine), or if the entry is for revision of a previously-learned routine.

a. For learn routines you are presently compiling (performing a learn routine on) for the first time, press the **INSert** key.

b. For previously-compiled routines, you may now **REVise** or **DELete** the **BRD/IC** index that is presently accessed. Refer to "Editing Previously-Learned Routines" instructions contained in this section.

15. The tester is now ready to accept an IC generic number entry. The tester displays the following prompt:

Display Prompt:
(**ENTER IC # 74:**)

16. Select IC family (type) that matches family of IC presently being learned using **Library Select** and **Input Level** key.

17. Using the **Scan** keys or **keypad**, enter the IC generic number. Press **Enter** key to verify entry.

18. If the IC generic number or family entry is not as intended, press the **Clear Entry** key. This will not cause a return back to the initial stage of the routine; simply enter IC generic number suffix digits again and press **Enter.** The **BRD/IC** index numbers are retained.

19. Board (**BRD**) index, IC (**IC**) index, and IC generic number entry is now complete and is indicated by the following prompt:

Display Prompt:
(**RDY TO RECD** 74153)
74153 = example IC number entered

20. Press the **TEST** key.

21. IC response is now recorded (learned) by tester and stored in RAM, as indicated by the following prompt:

Display Prompt:
(STORED)

22. After about 3 seconds, the tester returns to the **IC** index number entry stage of the procedure (step 12). Repeat steps 13 through 21 for other IC index entries (BRD/**IC**) if indexing under present board index number is desired.

23. To start a new board index number (**BRD**/IC), press either **Mode Clear** or **Clear Entry** and go to step 9. Repeat procedure for other entries.

24. Permanently store routine using custom program EEPROM (see MEMORY TRANSFER and CONTROL section).

25. Same-type circuits may now be tested using the **board learn** routine. Refer to BOARD TEST MODE section contained in this manual.

26. Press the **Mode Clear** key to allow for mode change.

EDITING PREVIOUSLY-LEARNED ROUTINES

The tester has provisions for selectively revising or deleting individual entries of a previously-learned routine without affecting other entries of a routine.

CAUTION

If the routine that requires REVision or DELetion is stored on an external EEPROM (EEPROM other than Socket #1 or #2), ***TURN POWER OFF*** *before installing EEPROM in one of the four* ***CUSTOM PROGRAM SOCKETS.***

REVising Previously Learned Routines

Example:

A previously-learned board learn routine has index **BRD 1/IC 15** containing IC generic number "7405". A design change on the board changes the IC under this index to IC generic number "7407". To reflect this change in the board learn routine and keep the routine up-to-date for that board, REVise is selected after the index is accessed.

REVise an earlier entry using the following steps:

1. Power-up the tester. Select **Board Learn** using **Mode Select** key.

2. Connect the **IC Test Clip** to the IC requiring revision. Make certain **PIN 1** marker on test clip corresponds to pin 1 of reference IC.

3. Connect the ⏚ **clip** to a chassis ground point on the reference (host) circuit.

4. Disable all clocks on reference circuit.

5. Power-up reference circuit possessing circuit revision(s).

6. Press the **RAM Clear** key.

7. Load the EEPROM that contains the routine requiring revision into the tester RAM (refer to MEMORY TRANSFER and CONTROL section contained in this manual).

8. Access the previously-compiled **BRD/IC** index that you desire to revise using the **Scan** keys or **keypad.**

9. Press the **Enter** key.

10. At this point, the tester is at the same point in routine as when the entry was initially entered. The tester issues the following prompt:

Display Prompt:
INS/REV/DEL ?

11. Press the **REVise** key.

12. Enter the revised IC generic number using the **Scan** keys or **keypad.**

13. When response of the revised IC is stored (storage immediately follows after **TEST** key is pressed), the revision is confirmed by the the following prompt:

Display Prompt:
(REVISED)

14. Make a record of the revision in BOARD LEARN/TEST LOG SHEET for edited routine.

DELeting Previously Learned Routines

Example:
A previously-learned board learn routine has index **BRD 11/IC 45** possessing generic IC number 7400. A design change on the board omits this device. To reflect this change in the board learn routine for that board, DELete is selected.

DELete an earlier entry using the following steps:

1. Power-up tester. Select **Board Learn** using **Mode Select** key.
2. Press the **RAM Clear** key.
3. Load the EEPROM that contains the routine requiring revision into the tester RAM (refer to MEMORY TRANSFER and CONTROL section contained in this manual).
4. Access the previously-compiled **BRD/IC** index that you desire to delete using the **Scan** keys or **keypad.**
5. Press the **Enter** key.
6. At this point, the tester is at the same point in routine as when the entry was initially entered. The tester issues the following prompt:

Display Prompt:
(INS/REV/DEL ?)

7. Press the **DELete** key.
8. When entry is deleted, the tester confirms the deletion and issues the following prompt:

Display Prompt:
(DELETED)

9. Make a record of the deletion in BOARD LEARN/TEST LOG SHEET for edited routine.

BOARD TEST MODE

The **Board Test** mode is where the actual testing of untested ICs is performed on circuits "learned" in the **board learn** mode. Since **BRD/IC** index numbers and IC generic numbers are stored in the learn mode, no keypad entry of index numbers, IC generic numbers, or IC family is necessary while testing in this mode.

NOTE
Refer to TIPS & HINTS TO HELP AVOID COMMON MISTAKES section of this manual before performing test for the first time.

The following **special prompts** may be encountered using this procedure. Consult SPECIAL PROMPTS section of manual if further information is necessary.

(Insufficient Vcc)

(NOT STORED)

(WARNING! INPUT EXCEEDS 16.5 V)

(TTL OVERVOLTAGE)

1. The tester RAM must contain a previously learned **board learn** routine. The tester RAM acquires the learn routine in either of two ways:

   a. Tester is still powered up from immediately-preceding **board learn** co-routine, thereby having the learn routine in RAM.

   b. Tester RAM acquires the learn routine by loading EEPROM into RAM. Refer to MEMORY TRANSFER and CONTROL section of this manual for instructions on loading routines.

2. Connect **IC Test Clip** to IC under test. Make certain pin 1 of IC under test corresponds to **PIN 1** marker on **IC Test Clip.**

3. Connect the ⏚ **clip** to chassis ground point on reference (host) circuit.

4. Power up the circuit under test.

5. Disable all clocks in circuit under test.

6. Set **Test Mode** to **Board Test** using **Mode Select** key. Tester is automatically set to **IN CKT** testing when this mode is selected.

7. Tester requests the board index number (**BRD/**) used in the **learn** co-routine, as indicated by the following prompt:

> Display Prompt:
> **(BRD)**

8. The **board index** from the corresponding **board learn** routine may be accessed in either of the following manners:

   a. Press and hold the **Scan ▼** key. The first (lowest) **BRD/IC** index number used in the **learn** routine will be accessed. At this point, pressing the **Scan ▲** key accesses the following **BRD/IC** index numbers. Using this method of entering the **BRD/IC** index number, the user is reminded of the IC generic number contained within the index pair, as shown with the following prompt:

> Display Prompt:
> **(BRD 1 IC 2: 74153)**
> 1= example **BRD/** (board index) number
> 2= example **/IC** (IC) index number
> 74153= example IC generic number

Press the **Enter** key to verify **BRD/IC** index entry.

b. If desired, **BRD/IC** index number can also be manually entered using the **keypad.** Enter the **BRD/** index number. Press **Enter** for correct entry. Press **Clear Entry** to clear wrong entry. Enter the **/IC** index number. Press **Enter** for correct entry. Press **Clear Entry** to clear wrong entry. When clearing either board or IC entries, tester only clears preceding entry.

9. After board and IC index entry is entered, tester displays the following prompt:

> Display Prompt:
>
> (RDY TO COMPARE)

10. Press the **TEST** key to test IC (compare against stored response).

> Display Prompt:
>
> (RESULT: PASS)

> Display Prompt:
>
> (RESULT: FAIL)
>
> (PIN: 4,8)
>
> 4,8= Pins where fault was detected. If arrow is present at right side of display, more pin faults were detected than could be presently displayed; press **Scan ⬆** key to access additional pin fault detections.

11. To retest the same IC again, press the **Retest** key, then **TEST** key.

12. To access additional **BRD/IC** index numbers, press the **Mode Clear** key and use **Scan** keys (or manually access index as described above) and access desired index on prompt.

13. Memory ICs will display the "PASS" or "FAIL" prompts listed above when tested in the **Board Test** mode. The checksum obtained during the learn mode is stored and used as a reference for a same-type untested IC.

14. Press the **Mode Clear** to allow for mode change. Select other modes using **Mode Select** key.

The tester allows the transfer of **board learn** routines between the tester RAM and permanent EEPROM memory. The tester performs the following memory control procedures:

1. **STORE:** Board learn routines compiled on the tester RAM can be transferred to permanent EEPROM memory using the **Store** key.
2. **LOAD:** Going the other direction, board learn routines stored in EEPROM can be returned to the tester RAM using the **Load** key.
3. **MOVE:** Using the **Load** key, **Store** key, and the tester RAM, board learn routines can be moved from one EEPROM to another.
4. **ADDING ROUTINES:** Newly-developed board learn routines can be added to an EEPROM which contain other previously-stored routines.

The abovementioned procedures are discussed individually in this section.

CAUTION

The following precautions will help avoid damage to the instrument.

1. Do not install or remove EEPROM from socket while tester is ON.
2. Install and remove EEPROM from socket only with ZIF socket levers in unlocked position (levers facing LEFT). Lock levers after EEPROM is installed.
3. Make certain EEPROM is correctly installed in socket before powering-up tester.

NOTE

Install only the following EEPROM types in the **CUSTOM PROGRAM SOCKETS:**

B & K-Precision part no. 308-363-9-001

Oki type MSM2816A RS-250

SEEQ type M2816A-30

XICOR type X2816A

Do not attempt use of other generic 2816A EEPROMs (such as Intel 2816A); write enable logic and timing parameters of these EEPROMs are not compatible with the tester.

The following **special prompts** may be encountered using memory transfer functions. Consult SPECIAL PROMPTS section of manual if further information is necessary.

Insufficient Space

Invalid PROM

RAM Empty

No PROM in socket

CUSTOM PROGRAM EEPROMs

For non-volatile, expandable storage of **board learn** routines, the tester is equipped with six EEPROM sockets. Two sockets (EEPROM socket numbers **1** and **2**), located inside the tester, are factory-equipped with 2k x 8 EEPROMs. Four easy-access **CUSTOM PROGRAM SOCKETS** are located in the **EEPROM Compartment** (EEPROM socket numbers **3** through **6**), allowing the user to increase the storage capability of the tester by installing additional EEPROMs. The socket number of any user EEPROM, correspondingly, is also the respective address number of the EEPROM IC. For example, an EEPROM in **CUSTOM PROGRAM SOCKET #4** is addressed during **Load** and **Store** by pressing "4" on the **keypad.**

EEPROM COMPARTMENT

EEPROM socket numbers 3 through 6 are located under a cover just above the **IC Test Socket.** Remove the compartment cover as described below.

1. Place a thumb at each lower corner of the compartment cover.

2. Using both thumbs, press the lower edge of the cover in. Cover will tilt up and away from instrument.

3. Reinstall cover by tilting cover into instrument in the same way as when removed.

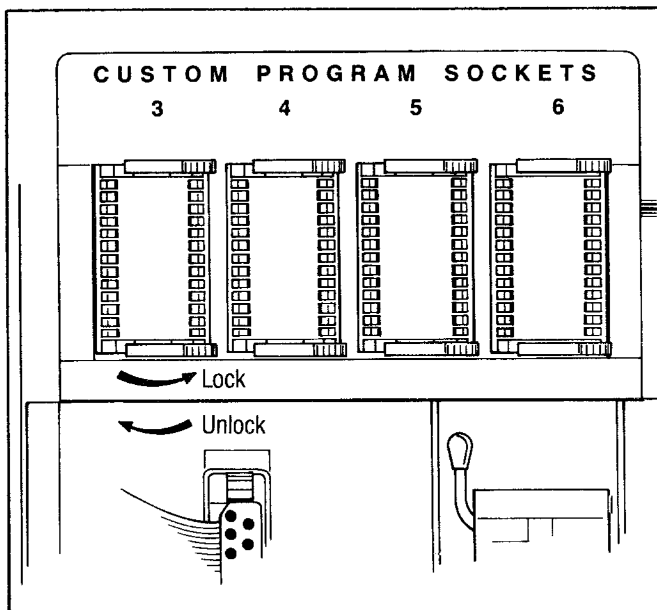


Fig 5. EEPROM Compartment.

STORING INTO EEPROM (STORE)

Learn routines, while in use, are held in the 2k x 8 tester RAM. **Therefore, the routine in progress will be lost if the tester power is turned off and the routine is not stored.** If it is desired to store a routine permanently, the routine can be **stored** in EEPROM. The following steps explain how to store a routine or routines (program) into EEPROM.

1. **Make certain EEPROM is installed in desired socket before starting a board learn routine.**

2. The tester RAM should contain the desired **board learn** routine in operating order, with any desired revisions already in effect.

3. Press the **Store** key. Tester prompts with the following message:

> Display Prompt:
>
> (SOCKET # 1-6 ?)

4. Enter the desired socket (address) number by pressing 1,2...through 6 on the **keypad.**

5. After entering socket number, the tester prompts with the following message:

> Display Prompt:
>
> (ARE YOU SURE ?)

6. If entered EEPROM socket number is as intended, verify by pressing the desired number again. If entered EEPROM socket number is not as desired, press **Mode Clear** and repeat steps 1 through 4 again.

NOTE

Answering "yes" to the "ARE YOU SURE?" prompt by pressing a socket number will **erase** the previous contents of the EEPROM. Be certain that valuable test routines will not be lost by an inadvertant store verification, due to pressing a socket number. The "ARE YOU SURE?" prompt is last chance to reject the store cycle. If you want to store (write) a routine on an EEPROM that already contains other **routines, do not** go through with store at this point. Refer to "Adding Routines to Previously-Written EEPROMs" instructions contained in this section.

7. When the entered EEPROM socket number is verified, tester prompts with the following message:

Display Prompt:

(STORING TO SOCKET 5)

5= example socket number

During the store cycle, the operating system locks out any other commands. The store cycle lasts about 30 seconds.

8. If a **store** operation is attempted with no EEPROM in position, the tester issues the following prompt:

Display Prompt:

(NO PROM IN SOCKET)

9. The tester has no provisions for software-based EEPROM contents cataloging or identification (ie; REM statements, headings, file catalogs). Therefore, the user should provide a means of identifying EEPROM program contents; stick-on labels placed over the EEPROM top surface are suitable.

NOTE

If you have used the optional "User Library Software" package to program custom devices into the Model 560, these new "user libraries" are also stored in Custom Program EEPROM. When a Custom Program EEPROM(s) is used as such, the EEPROM(s) are then unavailable for **board learn** storage; the affected EEPROM(s) must be "reconfigured". Refer to the USER LIBRARY SOFTWARE manual supplied with the User Programming kit for details.

LOADING EEPROM-BASED ROUTINE

The following steps explain how to recall (**LOAD**) a routine or routines (program) into the tester RAM.

1. Make certain the EEPROM containing desired routine is placed in desired EEPROM socket prior to powering-up tester.

2. Set **Test Mode** to **Board Test.**

3. Press the **Load** key. The tester may issue the following prompt:

Display Prompt:

(OK TO OVERWRITE RAM?)

4. This message alerts the user that a **board learn** routine is presently in RAM, and that routine will be **erased** if an EEPROM-based program is LOADed into the tester RAM.

   a. If you desire to save the RAM contents, reject the **LOAD** operation by pressing the **Clear Entry** key.

   b. If the contents presently in the tester RAM system can be deleted, press **Load** to continue. The tester now issues the following prompt:

Display Prompt:

(SOCKET (1-6)?)

5. At this point, enter the desired socket (address) number.

6. When the user EEPROM contents (board learn routines) are entirely transferred into the tester RAM, the tester prompts with the following prompt:

Display Prompt:

(LOAD COMPLETE)

7. Tester is ready for **board test** instructions. Refer to BOARD TEST MODE section contained in this manual.

MOVING CONTENTS BETWEEN TWO EEPROMs

Using the RAM as a temporary holding space, the contents of one EEPROM can be moved (transferred) to another EEPROM. This is useful when routines have accumulated on the internal, factory-installed EEPROMs (socket numbers 1 and 2) and you desire to keep these EEPROMs clear and available for use at any instance. Since the RAM and each EEPROM are of identical capacity (2k x 8), there is no chance of not completely moving the contents from one EEPROM to another. Use the following steps to perform EEPROM-to-EEPROM move.

1. Before powering-up tester, make certain source and destination EEPROMs are in the desired sockets.

2. Power-up the tester.

3. Press the **RAM Clear** key if tester was in other use prior to this procedure.

4. Load the source EEPROM into RAM:

   a. Press the **Load** key.

   b. Enter **socket number** of **source** EEPROM using **keypad.**

   c. Wait for **LOAD COMPLETE** prompt. The RAM now holds the source EEPROM contents.

5. Now store the RAM (source) contents into **destination** EEPROM:

   a. Press the **Store** key.

   b. Enter the desired **socket number** of the **destination** EEPROM using the **keypad.**

   c. Press number again to verify selection.

   d. Wait for store to complete, as indicated when prompt reverts to **BRD** prompt.

ADDING ROUTINES TO PREVIOUSLY-WRITTEN EEPROMs

Storing from RAM into a user EEPROM causes the EEPROM being stored into (destination EEPROM) to be written over entirely by the RAM contents presently held. Therefore, "new" routines compiled in RAM cannot be directly "added to" previously-compiled routines based in EEPROM. To add "new" routines in RAM to an EEPROM that already contains desired routines, use the following instructions:

1. Power-up the tester.

2. Load the destination EEPROM (EEPROM that contains "old" routines) into RAM. Refer to "Loading EEPROM-based Routine" instructions contained in this section.

3. Perform desired board learn routine(s).

4. When the board learn routine(s) is completed, the RAM will contain previously-learned routines as well as the recently-compiled routine(s), thereby effecting the "adding" of "old" routines with "new" routines.

5. Now store the RAM contents back into the destination EEPROM. Refer to "Storing into EEPROM" instructions contained in this section.

The Model 560 Programmable IC Tester is furnished with an RS-232 port, which is located on the instrument rear panel. The port is intended for connection to a personal computer, running the optional "User Library" programming software; or for connection to a printer.

CAUTION

Only connect the port to equipment designed for termination into an RS-232 port.

USING PORT WITH A PERSONAL COMPUTER

For connection to a personal computer using the optional software package, refer to the USER LIBRARY SOFTWARE manual supplied with the User Programming Kit.

USING PORT WITH A PRINTER

The port is compatible with printers with the characteristics listed below:

Connector Configuration:
Standard RS-232C DCE.
Pin 3: RxD (data TO printer).
Pin 4: RTS (ready from printer).
Pins 1, 7: Ground.

Parameters:
Baud Rate: 300 Baud, 1 start bit, 2 stop bits, 8 data bits. No parity bits, ASCII format.

Most standard printers (including those typically used with personal computers) accept the abovementioned parameters. A simple dot-matrix printer suited for use with the Model 560 is listed below:

Weightronix IMP-24

The following steps explain how to use the RS-232 port for printing data and test results.

1. Connect the printer to the **RS 232 Port Connector.**

2. If print is desired, press the **Port ON/OFF** key.

3. If port usage is attempted without a printer connected to the tester, the tester responds with the following prompt:

Display Prompt:
(NO DEVICE CONNECTED)

Under this condition, the tester's normal routine becomes "locked out", thereby preventing any use. After a wait of about 1 second, the tester will resume normal operation automatically.

4. Perform desired test routines. The printer will then print entered numbers, directive prompts, and test results.

NOTE
When using a printer, press the **Mode Clear** key after the last test result is made. Some printers store their last line of print in a buffer. Pressing the **Mode Clear** key ensures that the last line of print (last test result) will exit the buffer and be printed.

5. Press the **Port ON/OFF** key again to turn off print when desired print is completed.

DATA PRINTOUT EXAMPLES

```
ENTER IC#: 7400
RDY TO TEST 7400
RESULT: PASS
```

(IC entered; passed test)

```
ENTER IC#: 7447
RDY TO TEST 7447
RESULT: FAIL
PIN: 3
```

(IC entered; defect noted at pin 3)

```
ENTER IC#: 74300
NOT IN THE LIBRARY
```

(IC entered; not contained in selected library)

```
BRD 1 IC 1
INS/REV/DEL?
ENTER IC#: 7445
RDY TO RECD 7445
STORED
```

(indexed board learn entry; entry INSerted and stored)

```
BRD 2 IC 5
INS/REV/DEL?
REVISED
```

(indexed revised in board learn routine)

```
BRD 1 IC 14
DRY TO COMPARE
RESULT: PASS
```

(indexed board test entry; passed test)

```
BRD 1 IC 2
INS/REV/DEL?
ALREADY STORED
```

(INSert entry attempted; index already assigned)

While using the tester, special prompts are displayed under certain conditions. Typically, these special prompts alert the user **a)** that execution of an invalid step has been attempted by the user. **b)** a condition has been encountered where the tester needs further information from the user. **c)** that the tester overvoltage protection system is in effect, with the tester advising the user to correct the condition before proceeding with a step. **d)** that a tester error exists. In all cases, error prompts are accompanied by a three "beep" aural alert. In the case of a user error prompt, **remedial action** advice is given where applicable.

Display Prompt:

(ALREADY STORED)

Prompt indicating user has attempted to assign a board/IC (**BRD/IC**) index number in a **board learn** routine that already has this index pair assigned.

Remedial Action:

Recheck board/IC index numbers using **Scan** keys. Choose different, unused (**BRD/IC**) index number.

Display Prompt:

(CAN'T RESET DEVICE)

Prompt indicating in-circuit test was aborted because IC could not be reset.

Remedial Action:

The tester resets ICs by toggling the reset (CLR) pin. If that action fails (due to CLR pin tied inactive), the tester tries clocking the device to the reset state. In the rare case that this also fails, the above prompt is issued. All clocks must be disabled when testing in-circuit. Also check that outputs or clock pins are not tied inactive.

Display Prompt:

(DIAGNOSTICS....FAIL)

Prompt indicating error within the tester.

Remedial Action:

Prompt may occur if tester is turned off, then on again without waiting at least 15 seconds. If prompt occurs, power-down tester and wait 30 seconds until turning on again. If this action does not eliminate message, write down error code that occurs with prompt and contact authorized service center.

Display Prompt:

(END OF LIBRARY)

Prompt indicating user has reached the bottom or top of library listing.

Remedial Action:

Usually, library end is reached when user attempts to access a device of a different family than is currently selected (for example, trying to scan directly from the 4000 family to the 40000 family. Make certain that **Library Select** is correctly set for the desired IC type.

Display Prompt:

(**Insufficient Space**)

Prompt indicating tester RAM is near full, and intended index entry will not fit.

Remedial Action:

Note last board/IC (**BRD/IC**) index currently in use. Store contents presently in RAM into blank EEPROM. Press **Clear RAM** key and continue with subsequent entries on cleared RAM.

Display Prompt:

(**Insufficient Vcc**)

Prompt indicating Vcc of in-circuit IC under test is below operating limit or not present at all.

Remedial Action:

Make certain host circuit of IC under test is powered-up with fully functional power supply. If using the **device compare, board learn,** or **board test** modes, and **OUT CKT** testing is desired, make certain that **IN CKT/OUT CKT** feature is set to **OUT CKT** at all times of the procedure.

Display Prompt:

(**INVALID PROM**)

Prompt indicating EEPROM in **CUSTOM PROGRAM SOCKET** is of incorrect type. Also appears if no EEPROM is in socket during memory **Load.** Also appears if EEPROM contains a "user library" created with the optional software package (refer to USER LIBRARY SOFTWARE manual).

Remedial Action:

Use only approved 2816A EEPROM (**B & K-Precision** part number 308-363-9-001; or other EEPROMs listed in MEMORY TRANSFER and CONTROL section of manual). Make certain EEPROM is installed in desired EEPROM socket.

Display Prompt:

(**NO PROM IN SOCKET**)

Prompt indicating socket called upon in memory **store** has no EEPROM installed.

Remedial Action:

Make certain EEPROM is installed in desired EEPROM socket.

Display Prompt:

(**NOT IN THE LIBRARY**)

Prompt indicating IC generic number accessed using **keypad** is not programmed into the tester library.

Remedial Action:

Make certain IC generic number is entered correctly. Eliminate possibility of incorrect or invalid IC generic number entry by using the **Scan** keys for IC generic number entry.

Display Prompt:

(**NOT STORED**)

Prompt indicating a board/IC index number pair (**BRD/IC**) was called upon in the **board test** mode that was not assigned (programmed) in the corresponding **board learn** routine; or that entire routine was not stored.

Remedial Action:

Make certain desired EEPROM is LOADed into RAM for the **board test** routine you want to use. Recheck record of board/IC index numbers used. **Scan** keys can be used in **board test** routine to check your choice of index numbers.

Display Prompt:

(**RAM EMPTY**)

Prompt indicating RAM is empty. RAM may have been cleared through two ways: **(a) RAM Clear** key was pressed. **(b)** Tester power was unexpectedly interrupted.

Display Prompt:

(**WARNING! INPUT EXCEEDS 16.5 V**)

Prompt indicating tester voltage sense feature is active, temporarily halting any further tester operation; tester is floated from in-circuit device.

Remedial Action:

Check host circuit Vcc for overvoltage condition (>16.5 V). Reset with **Mode Clear** key after overvoltage is corrected.

WARNING

The following instructions are for use by qualified service personnel only. To avoid electric shock, do not perform any servicing unless you are qualified to do so.

AC line voltage is present on line voltage input circuits any time the instrument is plugged into an ac outlet, even if instrument is turned off. Therefore, disconnect line cord before removing instrument cover.

FUSE REPLACEMENT

The tester is protected by a fuse located on the rear panel. If the fuse opens, this indicates a problem; the problem should be corrected before replacing fuse.

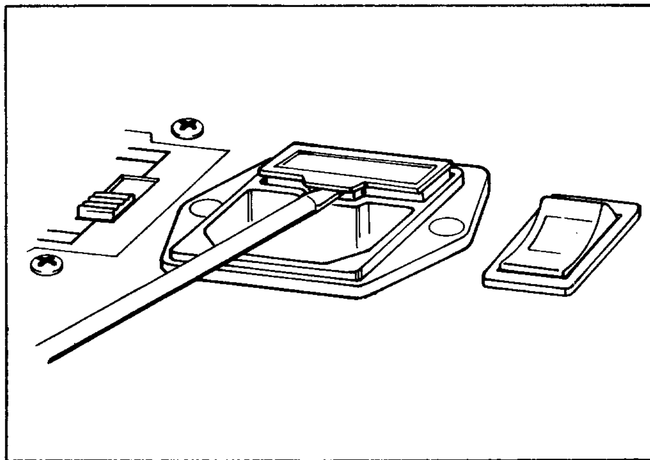


Fig. 6. Fuse Removal.

For 100/120V operation, replace a blown fuse with a 300 mA, 250 V, 5x20 mm slow-blow fuse only (**B & K-Precision** part number 194-018-9-001). For 220/240 V operation, replace blown fuse with a 200 mA, 250 V, 5x20 mm slow-blow fuse only. To remove fuse, disconnect line cord from **line cord receptacle.** The fuseholder is built into the **line cord receptacle,** thereby necessitating disconnection of line cord from the receptacle to gain access to the fuseholder. Insert a small screwdriver in the slot below the fuseholder. Pull fuseholder away from unit (as shown in Fig. 6) and replace fuse. A spare fuse is provided in the fuseholder, located behind the circuit fuse. Reinstall fuseholder by pushing fuseholder back into **line cord receptacle.**

INSTRUMENT REPAIR SERVICE

Being of digital design, no calibration or adjustment procedures are applicable or required for this instrument. Because of the sophistication of the instrument circuitry, only factory **B & K-Precision** service is recommended (other than procedures listed here). Return the unit **only** to the factory if service is needed. To use this service, even if the instrument is no longer under warranty, follow the instructions given in the WARRANTY SERVICE INSTRUCTIONS section of this manual. There will be a nominal service charge for the repair of instruments out of warranty.

LINE VOLTAGE CONVERSION

CAUTION

Disconnect line cord before changing line voltage switch settings.

The instrument can be operated on 100, 120, 220, or 240 V ±10%, 50/60 Hz sources. Line voltage selection is set using the **line voltage selector switches,** located on the unit's rear panel. As shipped, the switches are set to match the line voltage used in the country where the unit was shipped. Set the **line volt-**

age selector switches as required for other line voltage sources as shown in Fig. 7.

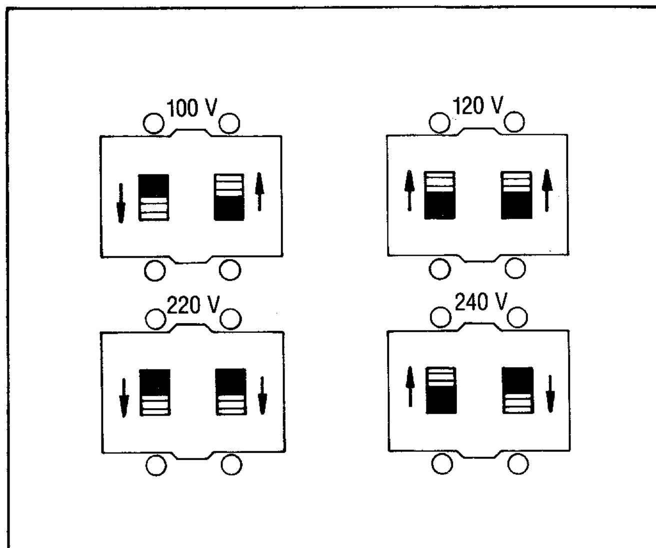


Fig. 7. Line Voltage Switch Settings.

COVER REMOVAL (Refer to Fig. 8)

1. Remove the four sheet metal screws on rear panel. The cover screws are located just above the edge of the plastic cover and screw into the metal chassis (approximately one inch below top edge of rear panel).

2. Remove the eight machine screws which fasten the cover to the chassis bottom. These screws are located one-half inch from the edge of the chassis, as shown in Fig. 8.

3. Lift cover straight up from instrument chassis. **Do not attempt to completely free cover from chassis at this time.** It may be necessary to shift cover while raising from chassis in order to clear ZIF socket and in-circuit test cable connector locking tabs.

4. Carefully disconnect keyboard flat-lead cable from chassis connector. Remove cover and place aside.

UPDATING LIBRARY/SYSTEM EPROMs

The tester IC library and operating system are contained on EPROM. As IC updates are compiled by our Engineering staff, updated EPROMs are periodically made available to our customers by **B & K-Precision.** The updated EPROM(s) is not merely an annex to the existing EPROMs in your instrument, but rather supersedes certain existing library EPROM(s). Therefore, certain existing EPROMs are discarded and replaced with updated EPROMs. The following instructions explain removal and installation of library EPROM ICs.

WARNING

Disconnect line cord before removing instrument cover.

CAUTION

Read procedure carefully before attemping EPROM replacement. Damage to instrument or EPROM can occur if EPROM is not installed correctly. Note the following instructions:

1. ***Do not** attempt procedure unless you are confident of performing this procedure competently and possess the proper tools.*

2. *Make certain correct EPROM IC is removed. Several physically-similar ICs are contained in the instrument.*

3. *Remove and install EPROM IC only with tool intended for removing and installing such devices.*

4. *Make certain all pins of the installed EPROM IC are inserted in their respective socket connections with no pins bent under IC package.*

5. *Make certain EPROM IC is fully inserted into socket.*

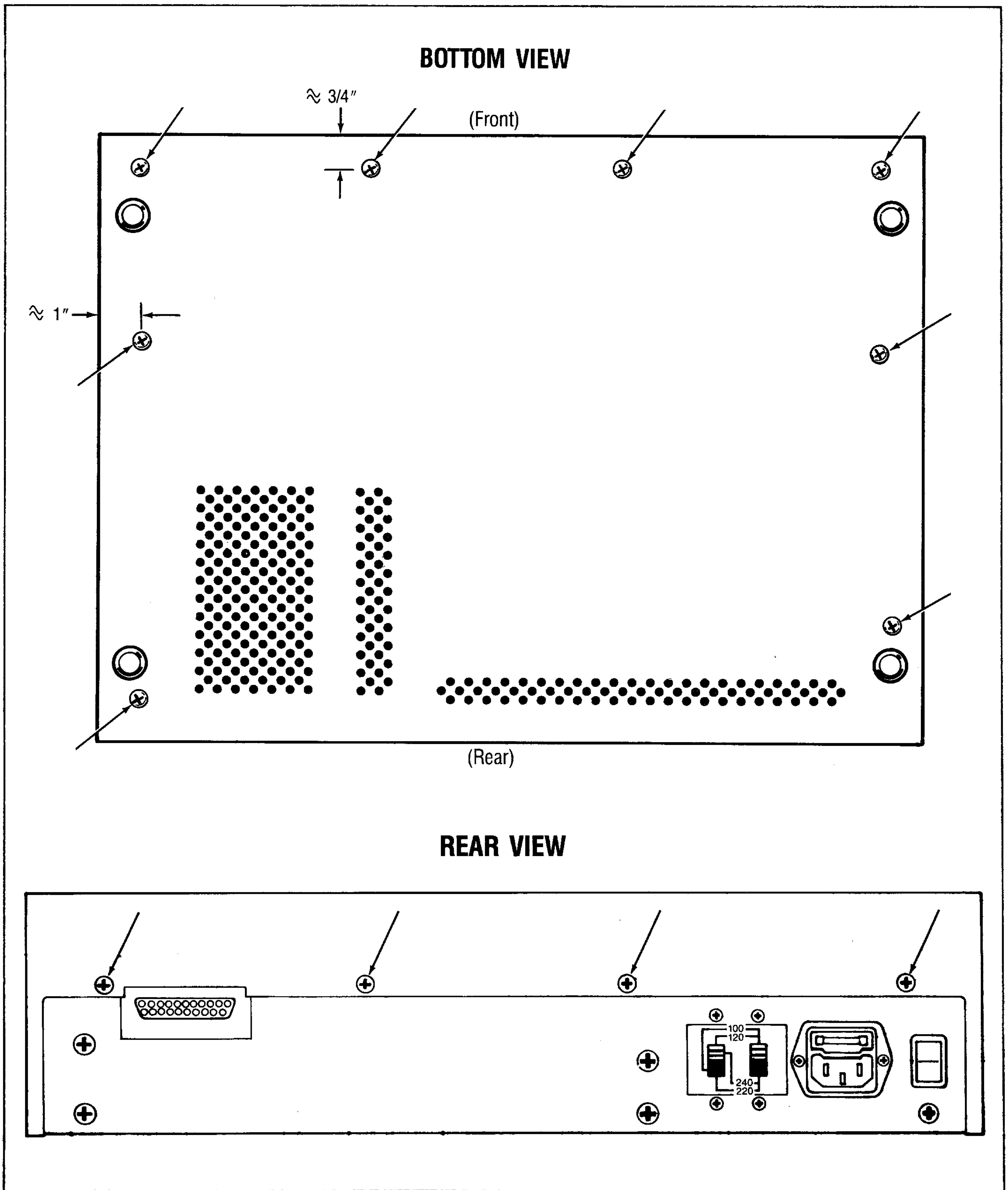


Fig. 8. Cover Screw Location.

EPROM REPLACEMENT

1. IC 4 through IC 8 constitute the IC library EPROM array. Your instrument is currently equipped with several of these EPROMs. EPROM ICs 5 through 8 are located about five inches right of the power supply, and two inches forward from the rear cover (as shown in Fig. 9).

2. EPROM update kits contain one or more EPROM ICs. These replacement update EPROMs will have the same identification labeling as the EPROMs currently installed in the instrument.

3. Using appropriate PROM extracting tool, only remove installed EPROM(s) which are to be replaced with update EPROM(s) kit. For example, if the received update kit contains an "IC 5" EPROM only, remove only IC 5.

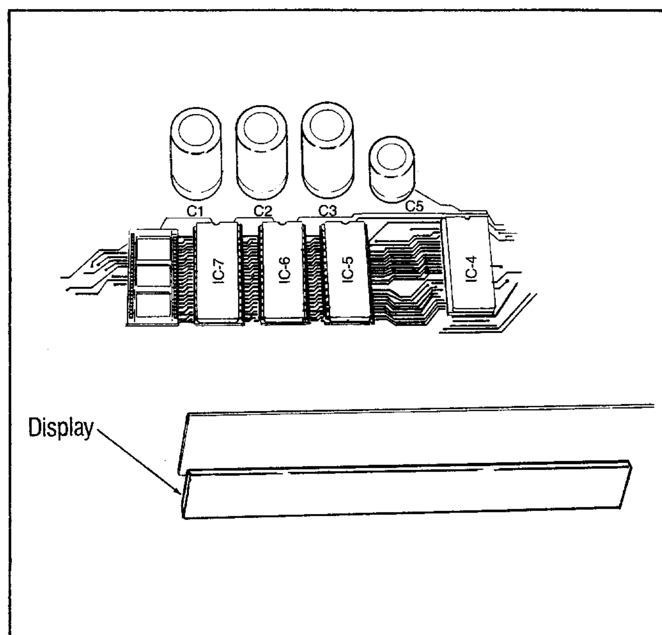


Fig. 9. Library EPROM Array.

4. Using an appropriate PROM installation tool, install updated EPROM(s). Note pin 1 correlation between EPROM IC and instrument socket (as shown in Fig. 10). **Make absolutely certain that all leads of EPROM IC are properly inserted into socket.**

COVER REPLACEMENT

CAUTION

Correct cover replacement is critical to avoid damaging the instrument. Follow instructions closely.

1. Place the ZIF **Socket Lever** in its "up" position (lever perpendicular to socket). Push both **Test Cable Connector** locking tabs towards each other.

2. Reconnect the keypad flat-lead cable. Place the cover on instrument while making certain of the following points:
   a. **Do not** reinstall cover screws at this point.
   b. Make certain that excess flat-lead cable is pushed back towards the main printed circuit board.
   c. Make certain that all LEDs (**Mode, Input Level,** etc.) align with their respective front-panel windows before refastening cover.
   d. Make certain that the cover does not interfere with the **IC Test Socket, Test Cable Connector,** or ⏚ **Connector.** All should align with their respective cover cut-out holes.

3. Reinstall the cover screws, tightening only a few turns. Tighten screws securely only after all screws are threaded into chassis.

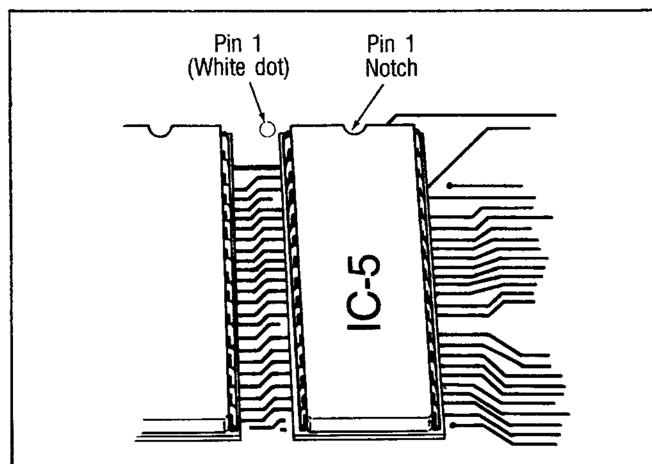


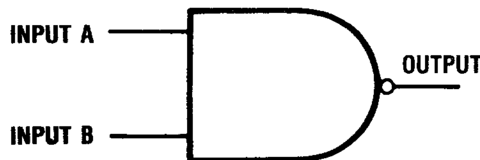
Fig. 10. EPROM Pin 1 Marker.

APPENDIX I: Why the Compare and Learn Modes are Often Necessary for In-Circuit Testing

HOW CONVENTIONAL FUNCTIONAL TESTS WORK

Conventional IC functional tests (such as the Out-of-Circuit Device Test Mode used with the Model 560, and those offered as the only test mode on conventional testers) test ICs by generating test patterns which exercise all possible input state combinations of the IC being tested. As an example, the two-input device shown in Fig. 1 has a maximum of four input-state combinations. These four possible input combinations yield four **test patterns** that the tester must carry out to completely test this device. When the four test patterns (① thru ④) and the device's resulting output are arranged in a table, a **truth table** is developed. As noted by the name, the truth table represents the response that should be obtained for test patterns ① through ④.

For the example IC in Fig. 1, conventional testers (as well as the Model 560 Device Test Mode) produce and execute each of the test patterns ① through ④, apply one pattern at a time to the inputs, and check the output result for each test pattern. The correct results for a given IC are known and are held in the tester's memory. The tester checks the results obtained from the IC under test by executing each test pattern and then decides if the results match the pre-determined correct results: If **all** of the obtained results agree with the pre-determined results, the IC is declared "good", or PASS. If **any** of the results **do not** match with the pre-determined correct results, the tester declares the IC "defective", or FAIL.



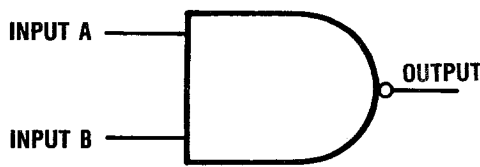
TRUTH TABLE

	INPUT A	INPUT B	OUTPUT
①	L	L	H
②	L	H	H
③	H	L	H
④	H	H	L

Fig. 1. Example Truth Table for 2-Input NAND Gate.

Fig. 2 shows the truth tables and comparisons between a good device (IC #1) and a defective device (IC #2). Note how on IC #2 test pattern ④ does not match the predetermined result. The tester notices the error and declares the IC as defective.

IC #1: "GOOD" IC

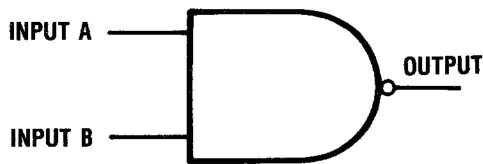


TRUTH TABLE

	INPUT	INPUT	GATE OUTPUT	TESTER REQUIRES:
①	L	L	H	H
②	L	H	H	H
③	H	L	H	H
④	H	H	L	L

H= +5 volts
L= 0 volts

IC #2: "DEFECTIVE" IC"



TRUTH TABLE

	INPUT A	INPUT B	GATE OUTPUT	TESTER REQUIRES:
①	L	L	H	H
②	L	H	H	H
③	H	L	H	H
④	H	H	**H**	**L**

H= +5 volts
L= 0 volts

mismatch

Fig. 2. Truth Tables of Gate Outputs vs. Pre-Determined Responses for "Good" and "Defective" Gate.

WHY CONVENTIONAL TESTING WON'T WORK IN MANY IN-CIRCUIT APPLICATIONS

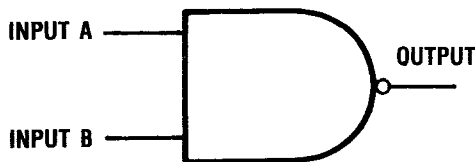
Conventional functional tests are perfectly suited for all out-of-circuit IC tests. With out-of-circuit testing conditions, the tester is free to toggle each input of the IC "high" and "low" as it pleases, thereby executing all patterns of the IC's truth table.

However, in many in-circuit applications, inputs of the IC are wired in ways which prevent the tester from executing the predetermined test pattern that corresponds to the IC's truth table. This is called "hard-wiring" and is commonly used.

Fig. 4 again shows a 2-input NAND gate with its inputs free from imposed states; in this case the expected, customary truth table can be executed and, as expected, the gate output exactly matches the response required by the tester (designated "TESTER REQUIRES" in all truth tables shown).

Fig. 5 shows the same 2-input NAND gate wired with Input A tied to Vcc (+5 volts). This is a very common "in-circuit" configuration. Assume that the gate is perfectly functional. Now, we'll attempt conventional functional testing of the gate. Notice what has happened to the test patterns. During the execution of test patterns ① and ②, Input A of the IC was prevented from going to the "low" (0 volt) state. **Most importantly**, notice what happened during test pattern ②: The tester tried to pull Input A low. However, Input A is tied to +5 volts. During test pattern ②, this condition prevented the **expected test pattern** from being executed. Therefore, in this case the **expected output** was not produced. Instead of a "high" IC output during this test pattern, the IC outputed a "low", causing the tester to declare the IC as "defective" even though the IC is known to be good.

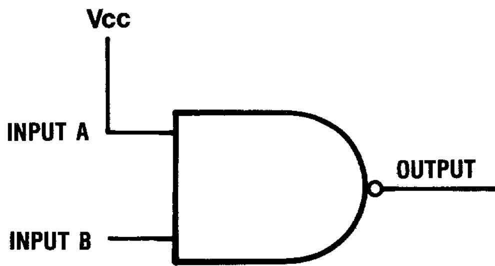
Fig. 6 shows the same 2-input NAND gate wired as an inverter; both leads are tied together. This is another very common "in-circuit" configuration. Again assume that the gate was previously checked and known to be good. Now, we'll again attempt conventional functional testing of the gate. Again, notice what has happened to the test patterns. During test pattern ②, Input A is expected to go "low" while Input B is expected to go "high"; but the jumper connecting the two inputs together makes opposite states on each input impossible. During test pattern ③, the opposite input state orientation occurs; but again, the jumper connecting the two inputs makes this impossible. During test patterns ② and ③, an **invalid** result is outputed from the gate. The tester will certainly give a "defective" result during test pattern ② or ③, or both. Again, due to the **unexpected, non-standard** input wiring, the tester will declare the IC as "defective" even though the IC was known to be good.



TRUTH TABLE

	INPUT A	INPUT B	GATE OUTPUT	TESTER REQUIRES:
①	L	L	H	H
②	L	H	H	H
③	H	L	H	H
④	H	H	L	L

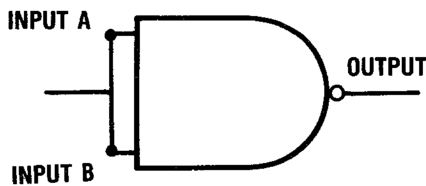
Fig. 4. Truth Table for 2-Input NAND Gate in Standard Configuration.



When one input is wired to Vcc, test patterns ① and ② are invalid because Input A cannot toggle "low".

	INPUT A	INPUT B	GATE OUTPUT	TESTER REQUIRES:
1	~~L~~ H	L	H	H
2	~~L~~ H	H	**L**	**H**
3	H	L	H	H
4	H	H	L	L

Fig. 5. Truth Table Showing Test Pattern Changes.



When both inputs are wired together, test patterns ② and ③ are invalid because Input A and B cannot attain opposite logic states simultaneously.

	INPUT A	INPUT B	GATE OUTPUT	TESTER REQUIRES:
①	L	L	H	H
②	L	H	**I**	**I**
③	H	L	**I**	**I**
④	H	H	L	L

I = Invalid state; could result in random H or L gate output.

Fig. 6. Truth Table Showing Test Pattern Changes.

HOW THE MODEL 560 COMPARE AND LEARN MODES TEST HARD-WIRED, IN-CIRCUIT DEVICES (When Conventional Testers Can't)

In the previous pages, the following points were made regarding conventional logic IC functional testing:

1. Conventional functional testing exercises the IC inputs using pre-determined logic patterns made available by the tester (either through software or hardware stored codes). As each logic pattern is exercised on the IC, the output is checked against a pre-determined "tested good" reference response contained in the tester. The Model 560 contains these pre-determined logic test patterns (and the corresponding responses) in its **IC Library.**

2. Conventional functional testing cannot test an IC in many in-circuit situations, due to the inputs of the device being "hard-wired" in a particular state. This situation prevents the tester from performing its expected, customary test pattern. Therefore, the tester yields a "tested defective" result even when the IC is good. Typically, well over 50% of actual in-circuit configurations are hard-wired in some fashion that prevents testing with conventional functional test patterns.

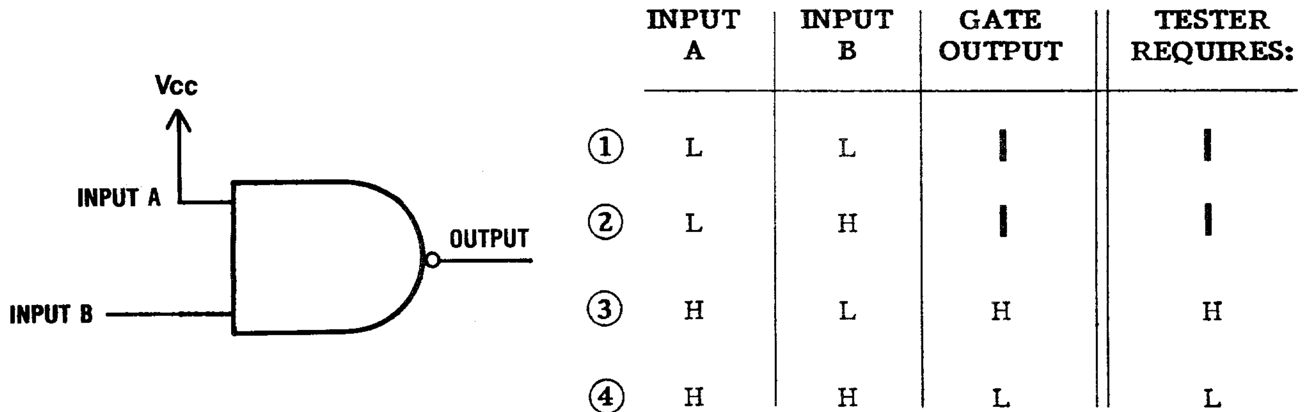
"A NAND GATE WITH ANY HARD-WIRED INPUT IS NO LONGER A NAND GATE"

A device's truth table is the "signature" of the device's function; when the device's truth table is altered through hard-wiring, a new function is created.

A non-standard wiring configuration which exemplifies a NAND gate whose truth table and function is altered through hard-wiring of inputs was shown in Fig. 5 and is used here again as the example in Fig. 7.

Fig. 7 shows the 2-input NAND gate with its standard truth table, with test pattern ② being disqualified as a condition which caused an error when using a conventional test. In other words, this was the test pattern that resulted in the NAND gate giving a "tests defective" result even though the NAND gate was good.

Now, say we have a NAND gate wired as shown in Fig. 7. Assume we know for a fact



	INPUT A	INPUT B	GATE OUTPUT	TESTER REQUIRES:
①	L	L	I	I
②	L	H	I	I
③	H	L	H	H
④	H	H	L	L

Fig. 7. In-Circuit NAND Gate with Disqualified Conditions.

that the circuit which contains the NAND gate, as well as the gate itself, is good. What if we could exercise the input with four test patterns and **store** whatever resulting output was obtained.

The obtained gate output would supercede the original truth table. In doing this, the standard truth table is of no importance and, therefore, is not used anymore: The obtained gate output will represent the "new" function of the NAND gate as wired in this example. This "new" gate output (response) develops a new truth table for the NAND gate; this "new" truth table is shown in Fig. 8.

Why do we store the response that resulted from the NAND gate and its "hard-wired" input? We store this response because this response serves as the **reference** for other NAND gates wired similarly.

This stored reference response is used exactly as the pre-determined response was used when testing out-of-circuit: This new stored response replaces the "tester requires" column in the truth table for the NAND gate and serves as the criteria which other NAND gates wired similarly will be tested upon.

Whatever output pattern that was created by the "hard-wiring" and stored will be the required output for other similar circuits (for this example, the circuit shown in Fig. 7).

	INPUT A	INPUT B	OUTPUT
①	L	L	I
②	L	H	I
③	**H**	**L**	**H**
④	**H**	**H**	**L**

Rejecting test patterns ① and ②, Compare Testing only considers...

the valid patterns ③ and ④ ...

	INPUT A	INPUT B	**TESTER NOW REQUIRES:**
new ①	H	L	**H**
new ②	H	H	**L**

These patterns yield the "new" Truth Table. The "new" patterns ① and ② will be used by the Model 560 Compare Mode to test additional "Fig. 7" circuits.

Fig. 8. Compare Testing Truth Table Transformed from Valid Test Patterns.

MODEL 560 LIMITATIONS

Any tester, regardless of its price, cannot test every IC in every situation. With capabilities to perform both in-circuit and out-of-circuit testing of over 500 generic TTL and CMOS digital ICs, the Model 560 out-performs all other IC testers in this price category. However, there are devices or configurations which the Model 560 will not test or which require special handling. These conditions are listed below.

1. In-circuit or out-of-circuit interface devices which require a negative power supply voltage. The Model 560 uses positive test voltages.

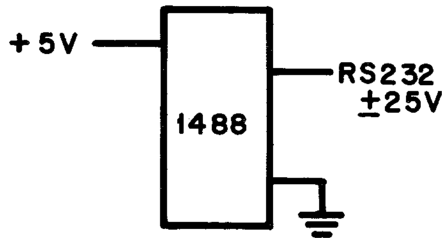
2. In-circuit or out-of-circuit monostable or voltage-controlled oscillators which require external components for operation. These devices cannot function without external components.

3. In-circuit applications where the output of the device under test is directly wired back to the device input. Such an example would be a D flip-flop with its $\overline{Q}$ output wired to the D input, as would be in the case of a divide-by-two counter. This condition prevents the tester from controlling the input independently from the output.

4. In-circuit applications where logic devices are used to drive LEDs and relays. Typically, these connections produce device output voltages which are within the "hysteresis" region of the tester (0.45 V - 2.4 V for TTL) and therefore, cannot be distinguished by the tester as verified logic "highs" or "lows".

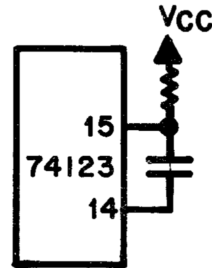
DIGITAL TESTERS CAN'T TEST THESE:

1 Dual-Polarity Translator Devices

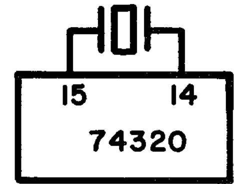


Line Driver; TTL-to-RS232

2 Devices Which Require External Timing Components (e.g., MMVs, PLLs, VCOs)

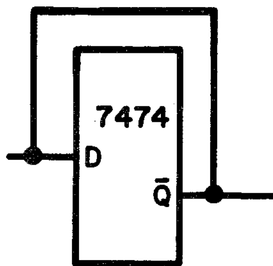


MMV



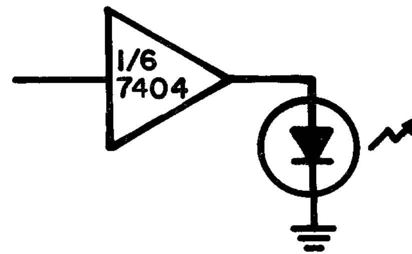
XTAL VCO

3 Sequential Devices Wired with Non-Resettable In-Circuit Configurations.

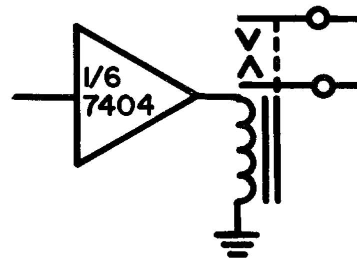


D-Type Flip-Flop with Output Directly Wired to Input.

4 In-Circuit Configurations with Lo-Z Loads.



Buffer Loaded-Down by LED Connected to Output.



Buffer Loaded-Down by Relay Connected to Output.

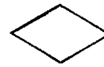
APPENDIX II: Flowcharts

This appendix contains flowcharts for the various tester procedures. These flowcharts provide the experienced user an efficient means of reviewing implementation procedure of the various modes, as well as providing a formatted method of training personnel to use the tester.

Due to the flexibility of the tester's software-based design, many variations are available to the user while using a particular test mode. However, a common organizational scheme has been designed for all test modes, which is reflected in the flowcharts.

The flowcharts use special symbolic representations to note the placement and applicability of the various commands and choices.

SYMBOL LEGEND


make user decision here

select function, mode, etc.

enter IC generic #; or BRD/IC #

Scan keys may be used at this point

Retest key may be used at this point.

display prompt

* If **OUT CKT** testing is used, set **IN CKT/OUT CKT** key= **OUT CKT** at this point.

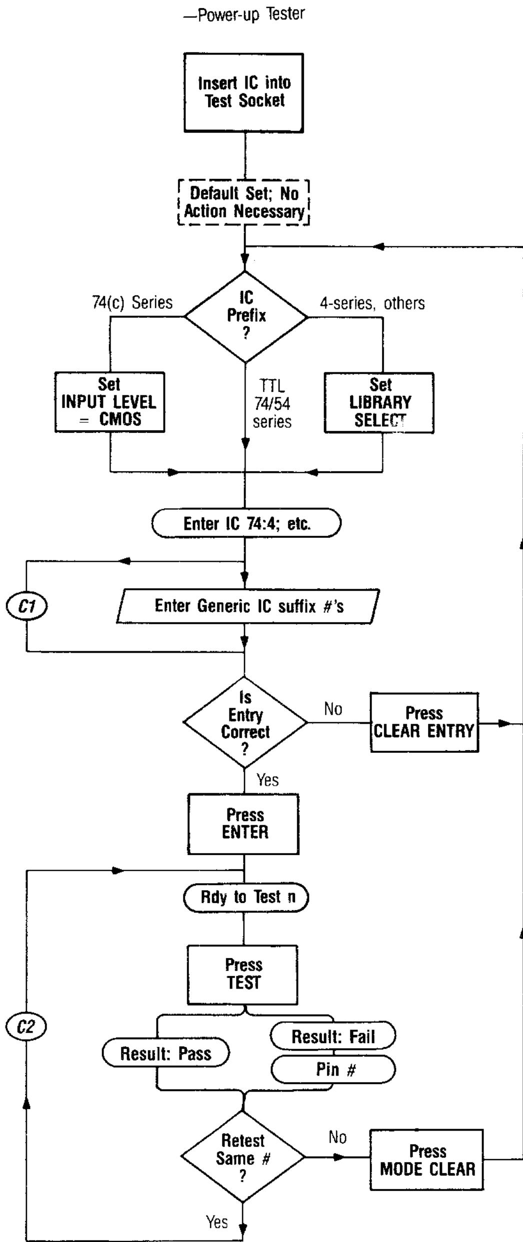


Fig. 1. OUT CKT Device Test Flowchart.

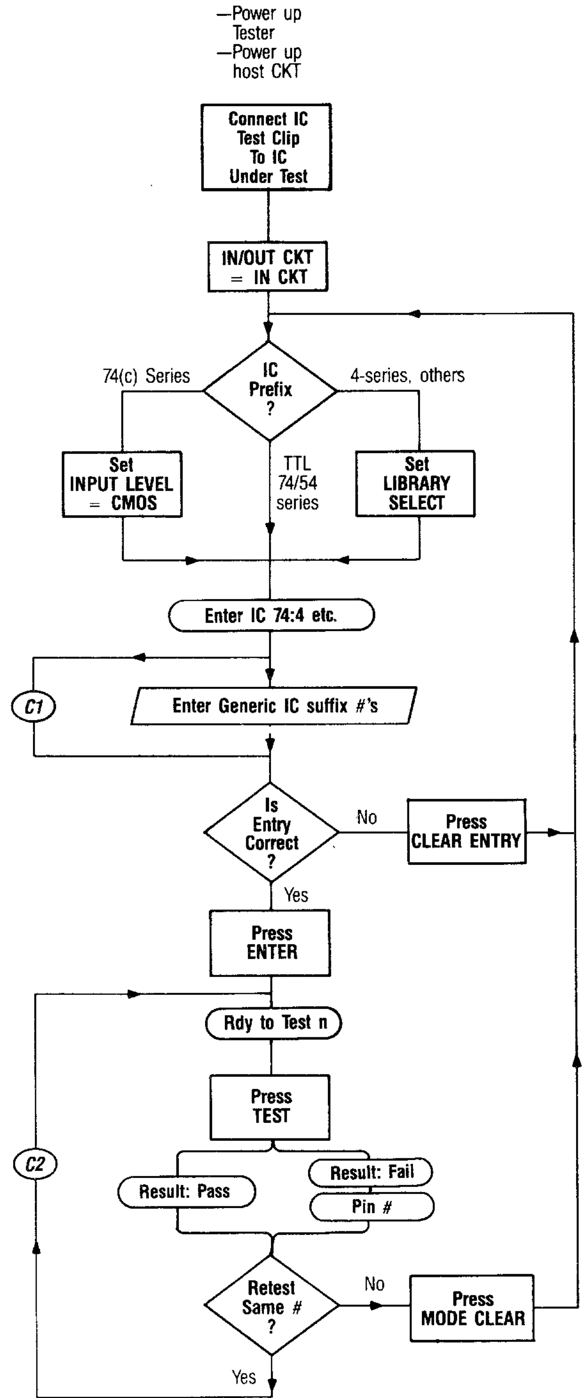


Fig. 2. IN CKT Device Test Flowchart.

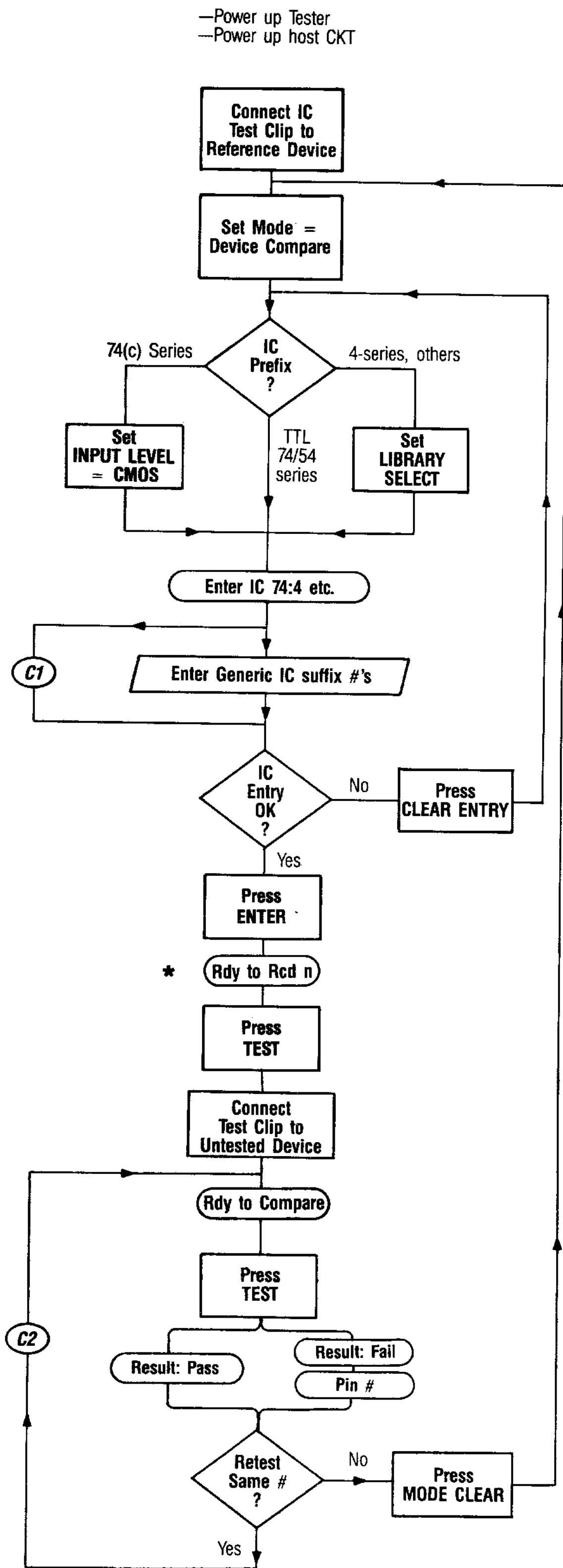


Fig. 3. Device Compare Flowchart.

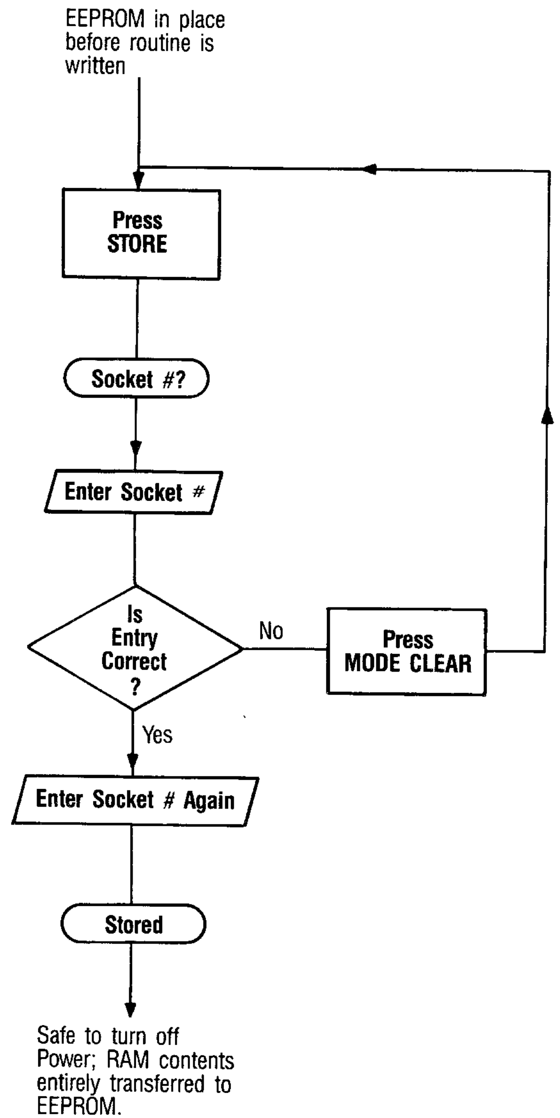


Fig. 4. Store Flowchart.

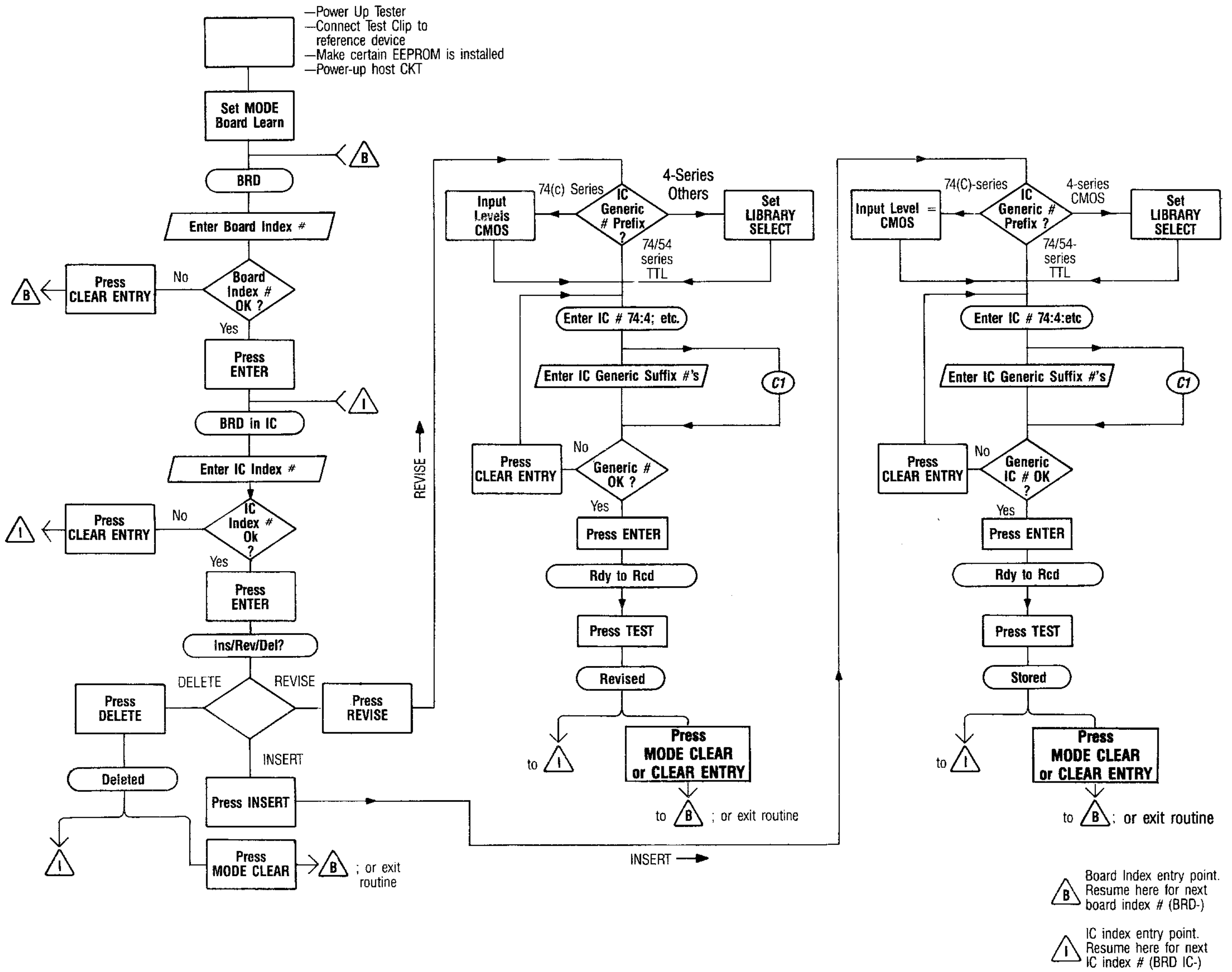


Fig. 5. Board Learn Flowchart.

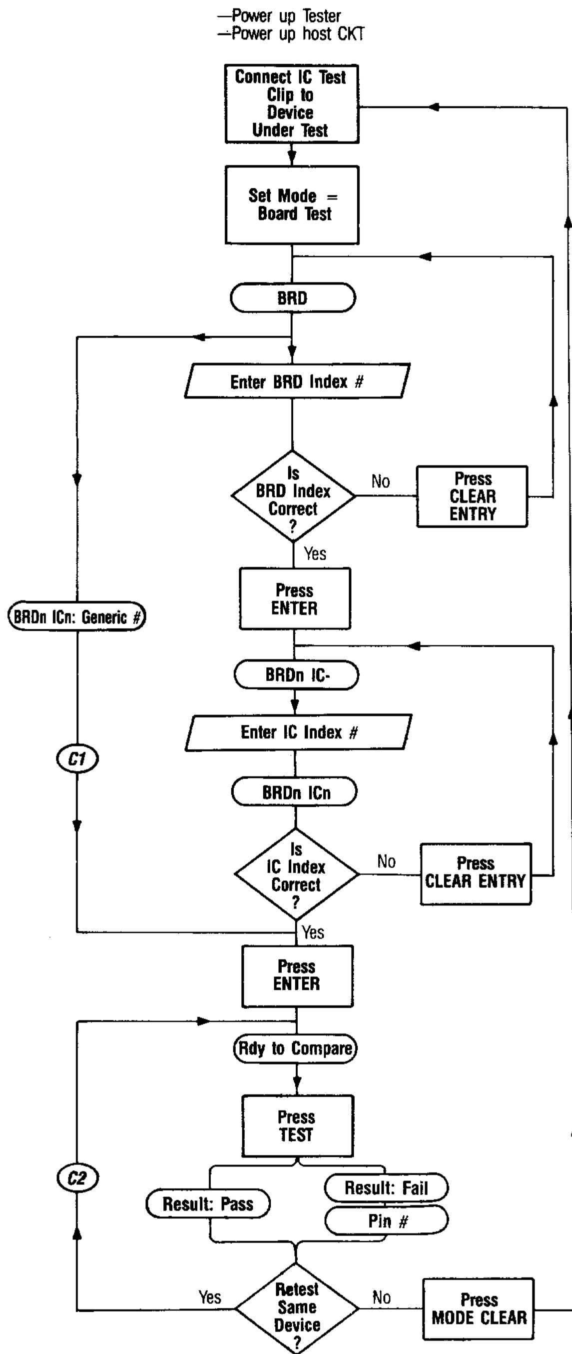


Fig. 6. Board Test Flowchart.

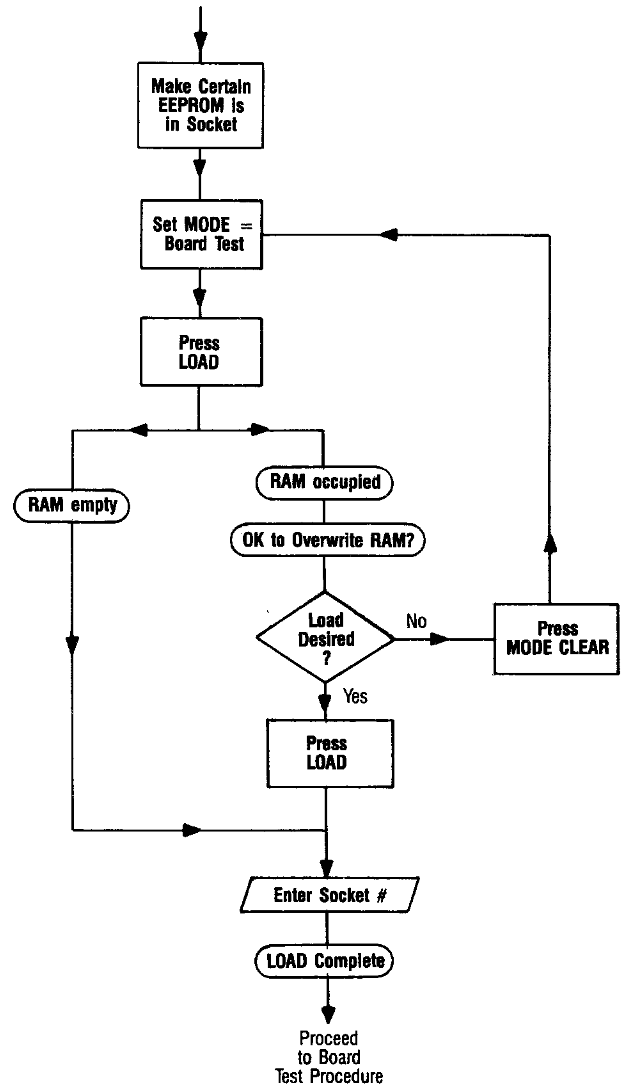


Fig. 7. Load Flowchart.