## MOS Memories

FUJITSU

# MB81C68-35, MB81C68-45

## 16,384-Bit Static Random Access Memory with Automatic Power Down

### Description

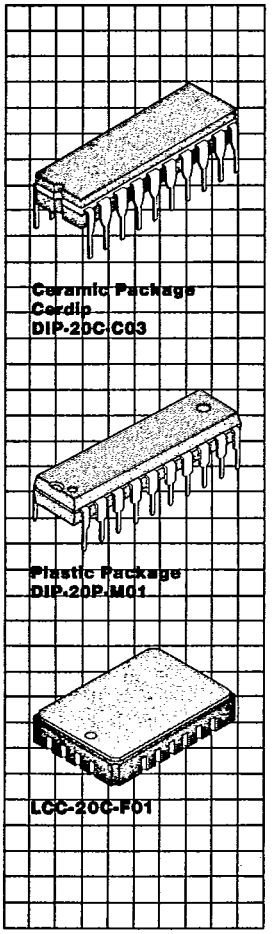
The Fujitsu MB81C68 is a 4,096 word x 4-bit static random access memory fabricated using C-MOS silicon gate technology. This device is fully static and requires no clock or timing strobe. All pins are TTL compatible, and a single +5 volt power supply required.

A separate chip enable ($\overline{E}$) pin simplifies multipackage system design. It permits the selection of an individual package when outputs are OR-tied. Furthermore, when selecting a single package by $\overline{E}$, the other deselected devices automatically power down.

The MB81C68 offers the advantages of low power dissipation, low cost, and high performance.

### Features

- Organization: 4,096 words x 4-bits
- Static operation: no clocks or timing strobe required
- Fast access time: TAVQV = TELQV = 35 ns max. (MB81C68-35) TAVQV = TELQV = 45 ns max. (MB81C68-45)
- Single +5V supply ±10% tolerance
- TTL compatible inputs and outputs
- Low power consumption: 385 mw max. (operating) 138 mw max. (standby)
- Three-state outputs with OR-tie capability
- Chip enable for simplified memory expansion, automatic power down
- All inputs and outputs have protection against static charge
- Standard 20-pin DIP package
- Pin compatible with Fujitsu MB8168



Ceramic Package
Cerdip
DIP-20C-C03

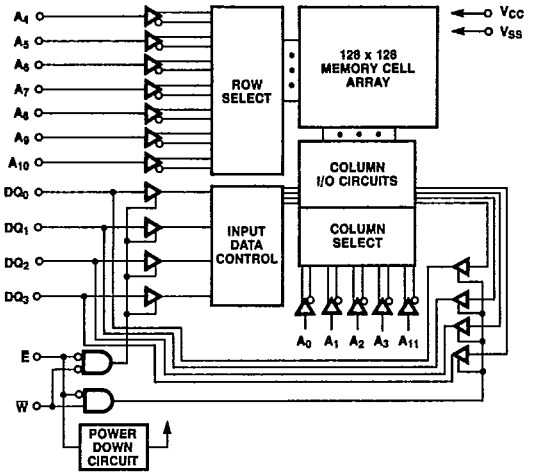
Plastic Package
DIP-20P-M01

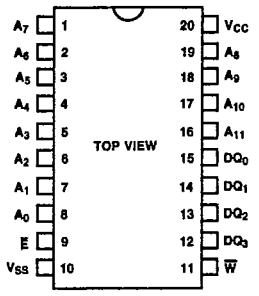
LCC-20C-F01

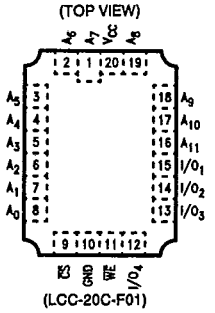
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

**MB81C68-35**
**MB81C68-45**

## MB81C68 Block Diagram and Pin Assignments




(LCC-20C-F01)

**TRUTH TABLE**

| $\overline{E}$ | $\overline{W}$ | MODE | DQ | POWER |
|---|---|---|---|---|
| H | X | NOT SELECTED | HIGH-Z | STANDBY |
| L | L | WRITE | $D_{IN}$ | ACTIVE |
| L | H | READ | OUT | ACTIVE |

## Absolute Maximum Ratings

(See Note)

| Rating | Symbol | | Value | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | −0.5 to +7 | V |
| Input voltage on any pin with respect to $V_{SS}$ | $V_{IN}$ | | −3.5 to +7 | V |
| Output voltage on any DQ pin with respect to $V_{SS}$ | $V_{OUT}$ | | −0.5 to +7 | V |
| Output current | $I_{OUT}$ | | ±20 | mA |
| Power dissipation | $P_D$ | | 1.0 | W |
| Temperature under bias | $T_{BIAS}$ | | −10 to +85 | °C |
| Storage temperature | $T_{STG}$ | Ceramic | −65 to +150 | °C |
| | | Plastic | −45 to +125 | |

**Note:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**
(Referenced to $V_{SS}$)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input low voltage | $V_{IL}$ | −0.5* | | 0.8 | V |
| Input high voltage | $V_{IH}$ | 2.2 | | 6.0 | V |
| Ambient temperature | $T_A$ | 0 | | 70 | °C |

**Note:** *−2.0V min for pulse width less than 20 ns.

**Capacitance**
($T_A$ = 25°C, f = 1 MHz)

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Input capacitance ($V_{IN}$ = 0V)* | $C_{IN}$ | | 7 | pF |
| DQ capacitance ($V_{I/O}$ = 0V)* | $C_{I/O}$ | | 7 | pF |

**Note:** *This parameter is sampled and not 100% tested.

**DC Characteristics**
(Recommended operating conditions unless otherwise noted.)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input leakage current | $V_{IN}$ = 0V to $V_{CC}$ | $I_{LI}$ | −10 | | 10 | μA |
| Output leakage current | $\overline{E}$ = $V_{IH}$, $V_{I/O}$ = 0V to $V_{CC}$ | $I_{LO}$ | −10 | | 10 | μA |
| Active (DC) supply current | $I_{OUT}$ = 0 mA | $I_{CC1}$ | | | 50 | mA |
| Operating supply current | $I_{OUT}$ = 0 mA, cycle = min | $I_{CC2}$ | | | 70 | mA |
| Standby supply current | $\overline{E}$ = $V_{CC}$ $V_{IN}$ = $V_{SS}$ or $V_{CC}$ | $I_{SB1}$ | | | 15 | mA |
| Standby supply current | $\overline{E}$ = $V_{IH}$ | $I_{SB2}$ | | | 25 | mA |
| Output low voltage | $I_{OL}$ = 8 mA | $V_{OL}$ | | | 0.4 | V |
| Output high voltage | $I_{OH}$ = −4 mA | $V_{OH}$ | 2.4 | | | V |

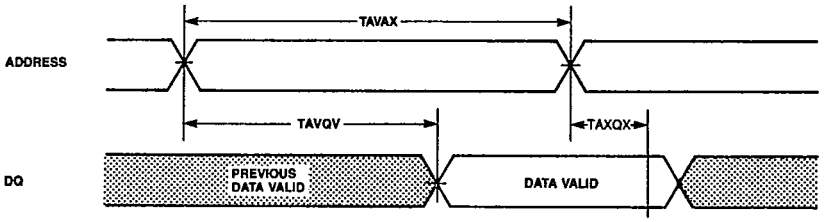
**AC Characteristics**
(Recommended operating conditions unless otherwise noted.)

**Read Cycle**

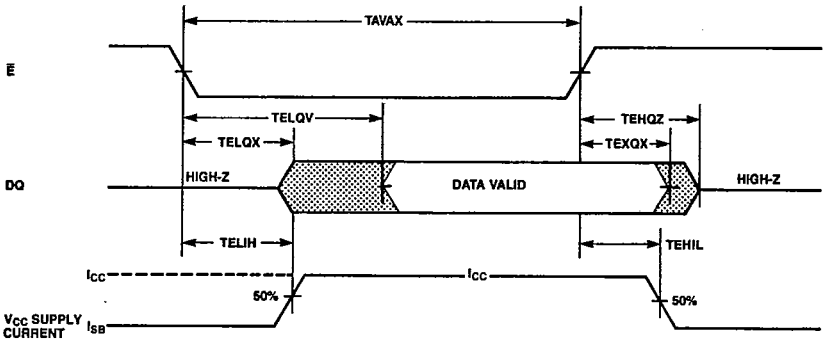
| Parameter | Symbol | MB81C68-35 Min | MB81C68-35 Max | MB81C68-45 Min | MB81C68-45 Max | Unit |
|---|---|---|---|---|---|---|
| Read cycle time | TAVAX | 35 | | 45 | | ns |
| Address access time | TAVQV | | 35 | | 45 | ns |
| Chip enable access time | TELQV | | 35 | | 45 | ns |
| Output hold from address change | TAXQX | 5 | | 5 | | ns |
| Output hold from $\overline{E}$ | TEXQX | 0 | | 0 | | ns |
| Power up from $\overline{E}$ | TELIH | 0 | | 0 | | ns |
| Chip enable to output in low-Z | TELQX | 5 | | 5 | | ns |
| Chip deselection to output in high-Z | TEHQZ | 0 | 15 | 0 | 20 | ns |
| Power down from $\overline{E}$ | TEHIL | | 30 | | 40 | ns |

**Read Cycle Timing Diagrams**[*1]

**Read Cycle: Address Controlled**[*2]




**Read Cycle: $\overline{E}$ Controlled**[*3]




NOTES: *1 $\overline{W}$ IS HIGH FOR READ CYCLE.
*2 DEVICE IS CONTINUOUSLY SELECTED, $\overline{E} = V_{IL}$.
*3 ADDRESS VALID PRIOR TO OR COINCIDENT WITH $\overline{E}$ TRANSITION LOW.

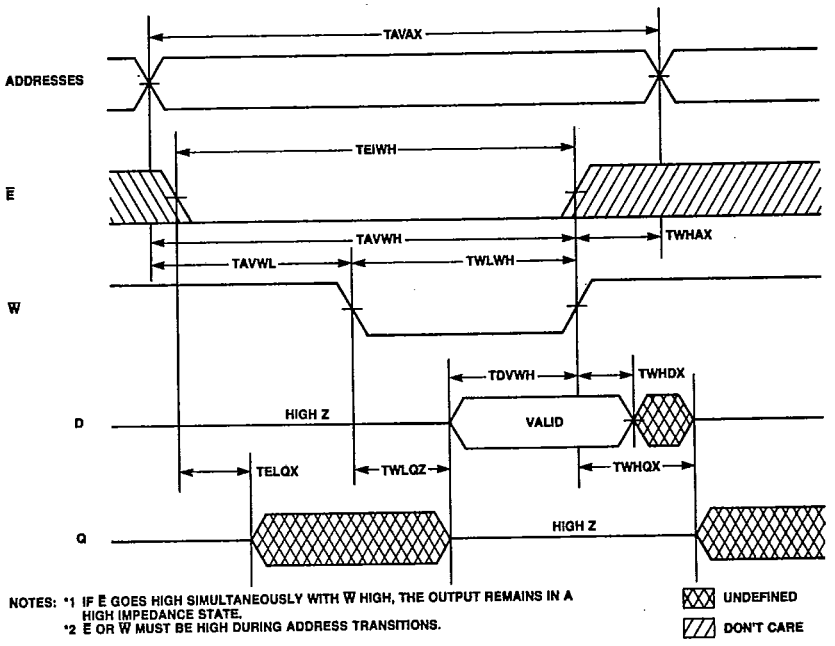
**AC Characteristics**
(Continued)
(Recommended operating conditions unless otherwise noted.)

**Write Cycle**

| Parameter | Symbol | MB81C68-35 Min | MB81C68-35 Max | MB81C68-45 Min | MB81C68-45 Max | Unit |
|---|---|---|---|---|---|---|
| Write cycle time | TAVAX | 35 | | 45 | | ns |
| Chip enable to end of write | TEIWH | 30 | | 35 | | ns |
| Address valid to end of write | TAVWH | 30 | | 35 | | ns |
| Address setup time | TAVWL, TAVEL | 0 | | 0 | | ns |
| Write pulse width | TWLWH | 30 | | 35 | | ns |
| Data setup time | TDVWH | 20 | | 20 | | ns |
| Write recovery time | TWHAX, TEHAX | 0 | | 0 | | ns |
| Data hold time | TWHDX | 0 | | 0 | | ns |
| Output high-Z from $\overline{W}$ | TWLQZ | | 15 | | 15 | ns |
| Output low-Z from $\overline{W}$ | TWHQX | 5 | | 5 | | ns |

**Write Cycle Timing Diagram**

**Write Cycle: $\overline{W}$ Controlled***1 *2



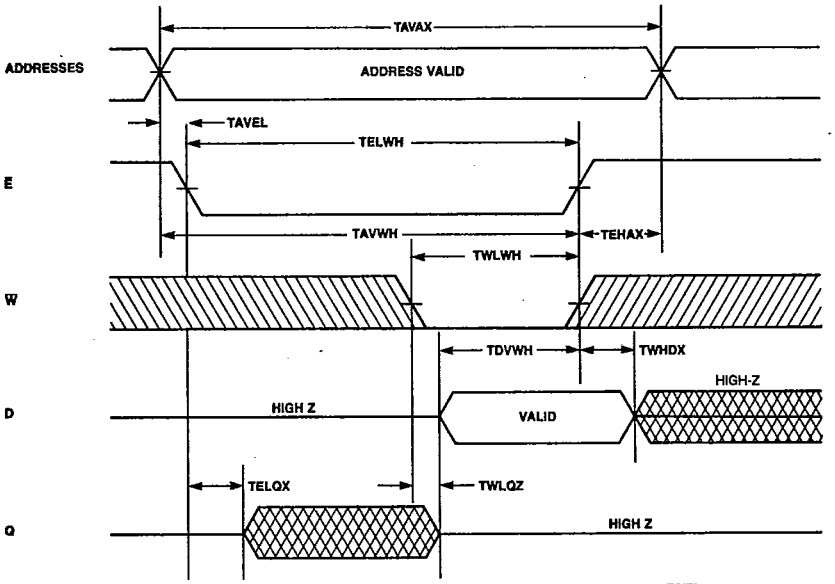

NOTES: *1 IF $\overline{E}$ GOES HIGH SIMULTANEOUSLY WITH $\overline{W}$ HIGH, THE OUTPUT REMAINS IN A HIGH IMPEDANCE STATE.
*2 $\overline{E}$ OR $\overline{W}$ MUST BE HIGH DURING ADDRESS TRANSITIONS.

**MB81C68-35**
**MB81C68-45**

**AC Characteristics**
(continued)
(Recommended operating conditions unless otherwise noted.)

**Write Cycle Timing Diagram**

**Write Cycle: $\overline{E}$ Controlled**[*1,*2]

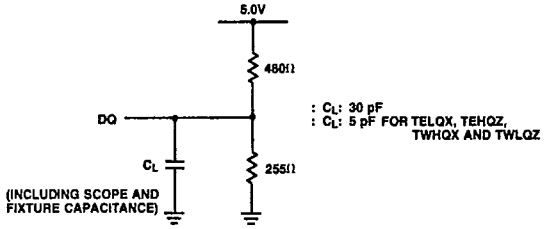



NOTES: *1 IF $\overline{E}$ GOES HIGH SIMULTANEOUSLY WITH $\overline{W}$ HIGH, THE OUTPUT REMAINS IN A HIGH IMPEDANCE STATE.
*2 $\overline{E}$ OR $\overline{W}$ MUST BE HIGH DURING ADDRESS TRANSITIONS.

**AC Test Conditions**

| | |
|---|---|
| Input pulse levels: | 0V to 3.0V |
| Input pulse rise and fall times: | 5 ns (Transient time between 0.8V and 2.2V) |
| Timing measurement reference levels: | Input: 1.5V |
| | Output: 1.5V |

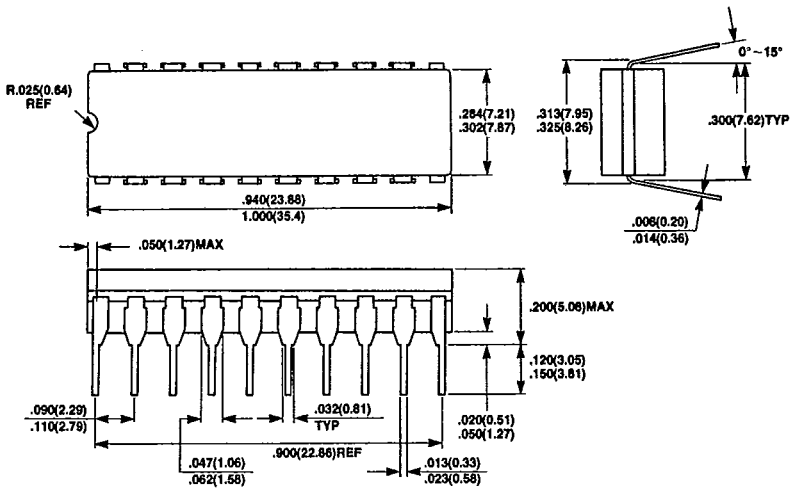
Output Load:



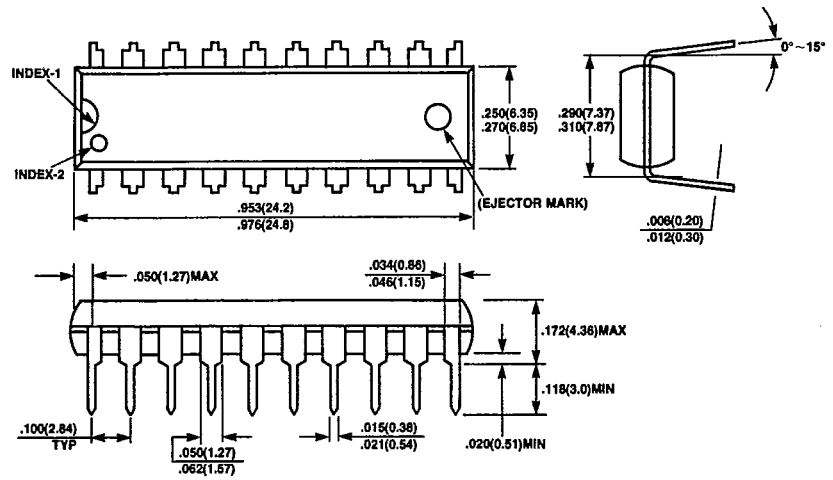
**MB81C68-35**
**MB81C68-45**

**Package Dimensions**
Dimensions in inches
(millimeters)

**20-Lead Ceramic (Cerdip) Dual In-Line Package**
**(Case No.: DIP-20C-C03)**

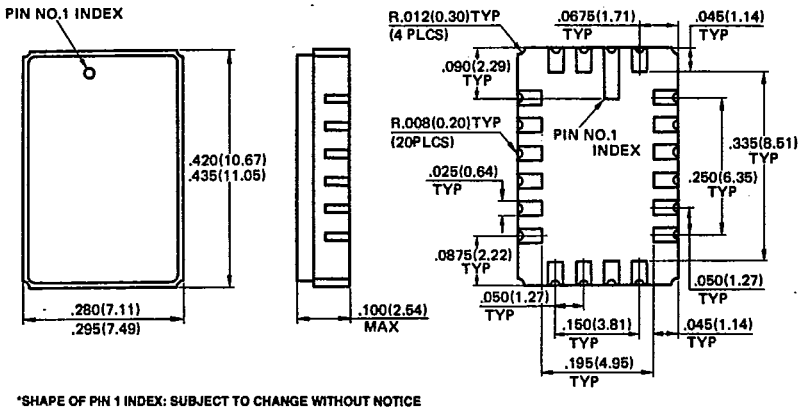



**20-Lead Plastic Dual In-Line Package**
**(Case No.: DIP-20P-M01)**



**Package Dimensions**
(continued)
Dimensions in inches
(millimeters)

**20-Pad Ceramic (Frit Seal) Leadless Chip Carrier**
**(Case No.: LCC-20C-F01)**




*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE